Stop that Leak

E-Beam Inspection Detects Crystal Defects Early in Device Fabrication

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An inline voltage contrast detection method utilizing an electron beam (e-beam) inspection tool and specially designed monitor structures is used to reveal crystal defects during the device fabrication process. The correspondence between bright voltage contrast defects and dislocations connecting the transistor source and drain is demonstrated using selective etching followed by SEM and TEM review. Finally, possible approaches to improve the capture rate of dislocations and their correlation to leakage current are discussed.

It has been widely reported that crystal defects can be very harmful in present-day silicon devices when they cause source-to-drain junction piping and subsequent transistor leakage. This failure is explained by anomalous dopant diffusion along the resistive path created by the defect. Defect formation is very often related to the isolation technology, which is responsible for the development of stress, and hence the generation and growth of dislocations. This effect becomes more and more important with shrinking device size and is dramatic when shallow trench isolation (STI) technology is used. It is necessary to identify a method to monitor the silicon crystal quality and to detect the formation of crystal defects at an early stage in the device fabrication process, in order to take the required corrective actions before the device is finished and tested.

Up to now, a combination of selective etching and scanning electron microscopy (SEM) inspection has been the only suitable methodology for identifying these crystal defects. This method has the disadvantage of being destructive and, in addition, it cannot be used for present-generation devices, both because of the reduced device size and because the increased dopant concentration confuses the etching results. This article describes how the KLA-Tencor eS31™ e-beam inspection tool can be used to detect and quantify crystal defects in the device fabrication process.

Experimental Details

Sample preparation: The monitor structures were fabricated using a non-volatile memory process flow, based on 0.13µm CMOS technology, using STI. The active area pattern was defined and etched to create the STI trenches, which were then filled by oxide deposition. After the active oxide growth, the gate electrode was defined. High dose arsenic and boron implantations were used to form the source and drain regions of n- and p-channel transistors, respectively. The implantation damage was annealed by a rapid thermal process (RTP). An oxide was deposited as the pre-metal dielectric; then the contacts were opened and filled with tungsten. The e-beam inspections were carried out at this step of the process flow. The process was completed with metal levels and passivation.

Structure description: Specific test structures for dislocation monitoring were designed to reproduce a critical pattern for dislocation formation and activation[1], consisting of transistor arrays with a high ratio (4:1) of active area corners to gates (figure 1). The rationale for this design is that the corner region of the active area pattern is the most critical in terms of mechanical stress: Two STI walls converge to an active

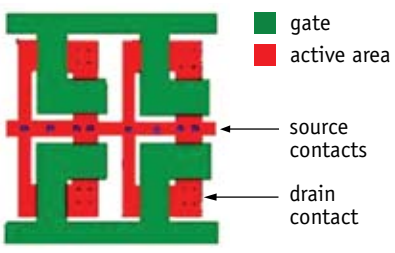

Figure 1: Test structures used for monitoring the formation of dislocations in the device process.

area corner region, and during oxidation the related stress fields superimpose in this region. Dislocations are most frequently observed close to the corners of the active area patterns[2], and structures with a high density of corners are prone to generating dislocations. The transistor array was designed with a common source region and individual drain regions, connected by parallel metal stripes as shown in figure 1.

This work concentrates on n-channel transistors, because it has been systematically observed that defects are formed in n-channel regions only. In previous works[2, 3] it was shown that dislocations nucleate in recrystallized amorphous regions produced by the high dose arsenic implantations that are used to form the source and drain regions of n-channel transistors. The formation of p-channel transistors does not involve amorphizing implantation; therefore, no dislocation defects are found in these regions.

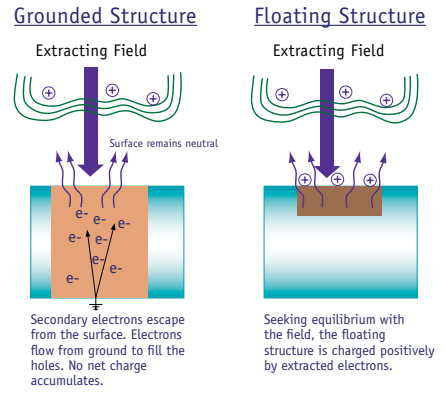

Figure 2: Simplified view showing principle of using extracting fields to capture crystal defects.

Experimental techniques: E-beam inspection provides a real-time electrical test with the capability to scan a wafer for systematic signatures or random electrical failures. When the e-beam strikes a defective floating structure that has a path to ground as a result of a sub-surface failure, the local area can no longer hold the charge. As a result, the local yield of electrons sensed by the system detector is changed, signaling a fault at that spot. The eS31 features a unique extended range of electron optics settings that enable adaptable e-beam current and landing energy for the materials being inspected. Moreover, a bias can be applied to the wafer so that the secondary electrons produced by the beam interaction can be either maintained at the wafer surface or extracted. This is a crucial capability for this study, since it determines the electrical behavior of the source and drain contacts when shorted by the resistive path of a dislocation (figure 2). In the case of the test structure that was investigated, there is no real path to ground; however, since all source contacts are connected, the source line acts as a virtual ground compared to the floating drain contacts.

Some potentially defective structures, as identified by the e-beam inspection, were prepared for microscopy analysis and investigated with conventional microscopy techniques: selective etching followed by SEM inspection and by transmission electron microscopy (TEM). In some samples, the layers above the silicon surface were removed by HF immersion, then received a selective etch (Secco d'Aragona[4]) to reveal defects, and the locations identified by the eS31 were reviewed by SEM. In other samples, a lamella for plan view TEM analysis was extracted at the locations identified by the inspection. A dual-beam focused ion beam (FIB) SEM was used to prepare TEM samples.

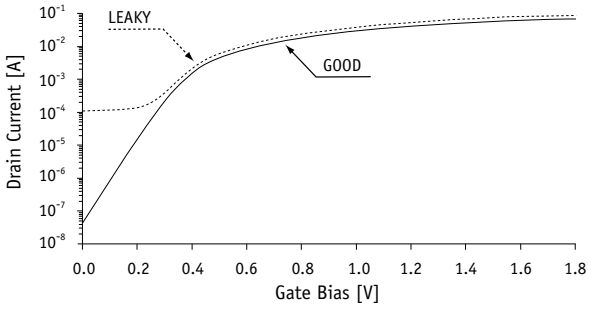

Figure 3: Transfer characteristics of a non-defective transistor array ("good"), and of a transistor array affected by dislocations ("leaky") connecting the source and the drain regions.

Dislocations are responsible for an increase in transistor leakage current under sub-threshold conditions (figure 3). To a good approximation, this comprises a source-to-drain current only, as the drain-to-substrate leakage current is negligible; hence, it is hereafter referred to as the "channel leakage current." In non-defective structures, the sub-threshold current shows the usual strong dependence on gate voltage and substrate voltage. On the contrary, in defective structures the channel leakage current is weakly dependent on both substrate and gate voltages. Hence, it is possible to choose measurement conditions that reduce the sub-threshold current below the leakage current contribution due to a single dislocation, making any dislocations easily detectable. Table 1 reports the

V_g(V)	0
V_d(V)	3
V_{sub}(V)	0
I_{nd}(A)	(1–3)10^{-8}
I^*(A)	10^{-7}

Table 1: Bias voltages used for measuring the sub-threshold current of the structures in figure 1, with resulting sub-threshold and limit leakage currents.

electrical measurement conditions used to test the dislocation monitor structures, including the typical sub-threshold current for non-defective structures, I_{nd}, and the limit leakage current value I*, above which the structure is assumed defective. Gate, substrate and drain voltages are also given.

Experimental Results

E-beam inspections: At the contact tungsten CMP layer, the e-beam inspector was optimized to enhance the voltage contrast signal[5]. A hyper-extracting field of 1500V was applied to reverse-bias the junctions, revealing strong bright defects wherever dislocations facilitate an electron path from the source line to the drain contact (figure 4). Signal-to-noise was so high (3.4) that a four-minute inspection was sufficient to detect defects on all test structures over the entire 200mm wafer.

Microscopy inspections: Figure 5 compares the inspector image of a transistor array showing a bright drain contact, and the SEM image of the drain region after delayering and selective etching. Dislocation etch features are clearly identified. Figure 6 shows the TEM plan view of a transistor with a bright drain contact. The TEM image confirms the presence of a dislocation connecting the source and the drain of this transistor. In addition, the microscopy analysis showed additional defects not revealed by e-beam inspection.

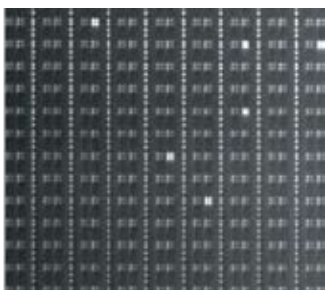

Figure 4: E-beam inspection image of a highly defective test structure showing multiple bright voltage contrast defects associated with dislocations.

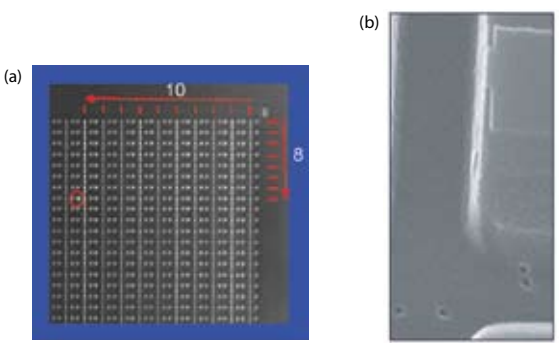

Figure 5: Voltage contrast image of a transistor array showing a bright drain contact (left), and SEM image after selectively etching the transistor (right).

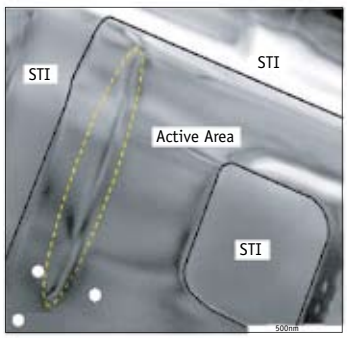

Figure 6: Plan TEM image of dislocation (highlighted by yellow circle) on a transistor with bright drain contacts.

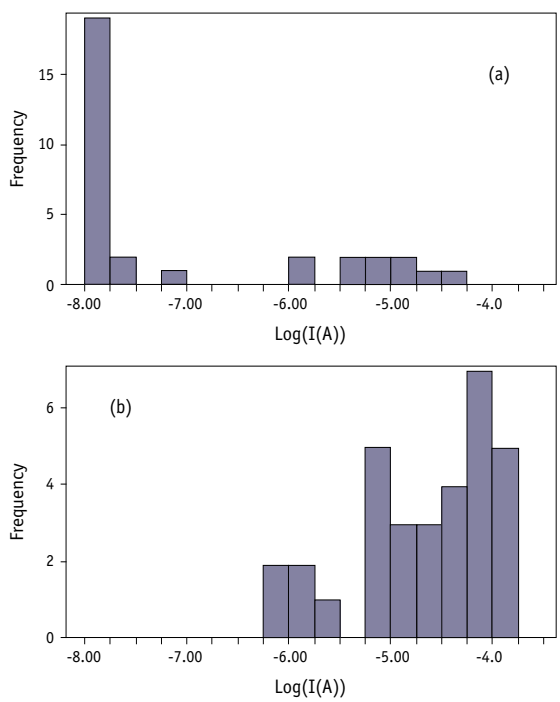

Figure 7: Leakage current histograms of a low-leakage wafer (top) and a high-leakage wafer (bottom).

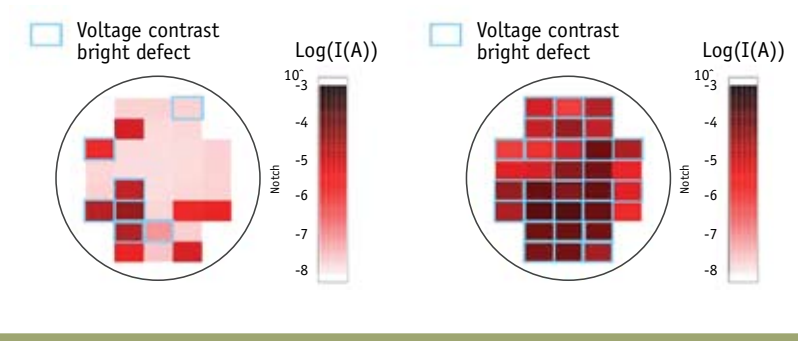

Figure 8: Superimposed leakage current maps and voltage contrast maps of a low-leakage (left) and a high-leakage wafer (right).

Electrical measurement results: Two wafers whose e-beam inspection results gave significantly different voltage contrast defect densities, also showed significantly different electrical performance. Figure 7 shows the leakage current distributions of the dislocation monitor structures in these wafers.

The leakage current maps of the dislocation monitor structures and the voltage contrast maps obtained by e-beam inspection were superimposed for comparison (figure 8). It is observed that the e-beam inspection can discriminate between the low leakage and the high leakage wafer, and also identify the leaky region in the low leakage wafer. It was observed that 80% of the leaky structures were identified by voltage contrast inspection. The remaining 20% were undetected because they lay within an uninspected care area border prescribed by cell-to-cell inspection on the eS31. Future work could increase the inspection area (and its correlation to electrical results) by either using die-to-die inspection, or upgrading to an eS32™, which reduces the care area border.

In some cases, a bright voltage contrast defect unrelated to source-to-drain leakage was also observed. Under hyper-extracting conditions, shorts to ground also appear as bright voltage contrast defects. The shorting can result from a previous-layer particle, residue or pattern defect. Systematic FIB review would confirm the nature of these defects.

Conclusions

Voltage contrast detection using an e-beam inspection system was established as an inline method to detect piping dislocations in devices at an early stage of the fabrication process. By using specially designed monitor structures, the correlation between bright voltage contrast events, and dislocations connecting the transistor source and drain was demonstrated by selective etching followed by SEM review and by TEM inspection. An 80% capture rate of the electrically defective defects was achieved, which could be further improved using a modified inspection strategy. Recent inspections on 65nm devices have confirmed the ability of e-beam inspection to detect dislocations under hyper-extracting conditions. This is promising for the 45nm node, for which strain-induced defects are expected to be among the biggest challenges.

Acknowledgements

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Inspections on 65nm devices confirm the ability of e-beam inspection to detect dislocations under hyper-extracting conditions.

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