Overlay control is a vital part of lithography in semiconductor manufacturing. Errors in the overlay of different lithographic levels can cause many electrical problems, thus impacting yield. Ultimately, you can shrink die size with better overlay control. Thus, economics dictates that overlay specifications must shrink along with device geometries, requiring continuous improvement in measurement and control.

HOW TO CHARACTERIZE OVERLAY ERRORS

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Overlay is defined as the positional accuracy with which a new lithographic pattern prints on top of an existing pattern on the wafer. Overlay measurement involves the design of special patterns used on two different lithographic printing steps such that a metrology tool can measure overlay errors at that point on the wafer. The older pattern in common use is the "box-in-box" (BiB) target, where an outer box is printed during the first lithographic step and an inner box is printed during the second pass (figure 1). Recently, a new target called AIM has shown superior measurement results. The AIM bars have much higher measurement precision and are immune to processing errors that can damage a traditional BiB target.

The goal of overlay data analysis is two-fold: assess the magnitude of overlay errors and determine, if possible, their root causes. Root cause analysis (extracting knowledge about your lithography process from the measured data) involves explaining the data with a model that assigns a cause to the observed effect.

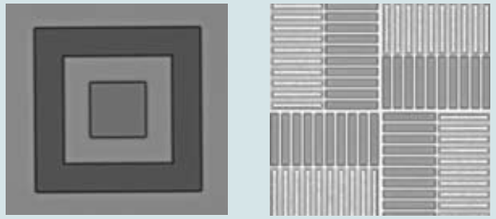

Figure 1: New AIM targets (right) demonstrate superior measurement results over typical BiB targets (left).

Consider three common sources of reticle overlay errors:

- Rotation of the reticle about an angle θ
- Translation, where the entire reticle field is shifted in x and y by Δx and Δy
- Relative magnification errors of ΔM_x and ΔM_y in x and y, respectively

Combining these sources gives this model for final overlay error:

$$dx = -\theta_x y + \Delta x + \Delta M_x x$$

$$dy = \theta_y x + \Delta y + \Delta M_y y$$

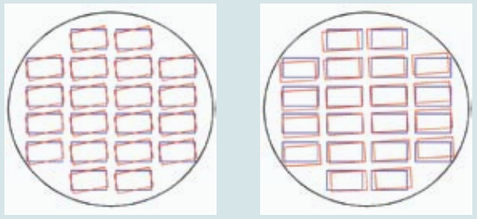

Figure 2: Different types of rotation errors as exhibited on the wafer: a) reticle rotation, and b) wafer rotation.

There are key differences between rotational errors applied to a reticle versus those applied to a wafer. Since the reticle field is repeated many times on one wafer,rotating the reticle is very different from rotating the wafer (figure 2). Similarly, a reticle magnification error (caused by the imaging tool) would yield a different signature than a wafer magnification error (caused by thermal expansion of the wafer). Translation errors, however, are exactly the same regardless of whether the offset is on the reticle or the wafer.

Measuring overlay errors is only one step in controlling overlay in a fab. By properly planning out the number and placement of the measurements to be made (sample planning), you can create a model to fit the resulting data such that the coefficients of the model represent physical error terms. These terms can then serve as correctables, which are fed back to the imaging tool to improve the overlay of the next set of printed wafers. The subsequent reduction in the total magnitude of overlay errors on the wafers results in major cost savings for a fab, while improving yield for a given design and allowing subsequent designs to shrink in size.

Chris Mack was Vice President of Lithography Technology for KLA-Tencor from 2000 - 2005. He currently writes and consults in Austin, Texas.

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