The Short Loop to Yield

Accelerating Flash Product Inspections using Electrical Defect Monitoring

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Floating gate word line structures on flash memory products have layouts that are uniquely suited to being tested using a special, high speed electron-beam inspection methodology previously confined to test structures. This article describes how Spansion's Fab 25 effectively used this approach to detect small physical defects that were causing a yield excursion in the cobalt silicide (Co_xSi_y) layer.

In the last few years, flash memory has emerged as the fastest growing segment in the memory market. NOR random-access flash is used in high-performance applications such as networking, cell phones, and games. NAND sequential-access flash is used primarily in mass-storage applications, such as digital cameras, personal digital assistants, and other products requiring memory cards. As consumers continue to demand innovative, small, fast, cheap products, flash memory fills the need for low-cost, low-voltage memory with reasonably fast read-write times.

As the largest company devoted to flash memory products, Spansion is under strong economic pressure to ramp its new products quickly, attain high yields, and achieve a fast time to market—all at the lowest cost possible. Part of the company's strategy is to detect and eliminate yield-critical front-end-of-line (FEOL) defects as quickly as possible during product development and ramp, and then to monitor defect levels in production to ensure that yield excursions are detected early.

In production, achieving low costs means monitoring defects using a high-throughput inspection system that can capture defects of interest (DOIs). While optical inspection systems normally perform cost-effective line monitoring, they do not easily detect some critical FEOL defect types. Very small physical defects, buried physical defects, and electrical defects can be detected only by using e-beam inspection.

When end-of-line testing at Spansion's Fab 25 in Austin, TX, encountered a yield excursion that the optical inspectors had failed to detect, a team of engineers began to investigate the problem using e-beam inspection. While the engineers were able to find the defects, which proved to be Co_xSi_y fibers less than 20nm in diameter that had shorted two Co_xSi_y word lines, scan times took a few hours because a small pixel size was required. It was clear that ordinary e-beam inspection was ineffective because it would significantly limit wafer-level sampling. Hence, an alternative approach was required.

The team recognized that the structure of the Co_xSi_y layer in which the fiber defects occurred mimics that of test structures from µLoop™, a non-contact electrical defect monitoring method developed by KLA-Tencor. µLoop uses specially designed test structures together with e-beam inspection to perform inline electrical tests. All defects detected by the method are necessarily yield-limiting, and because it detects the defects' electrical properties rather than their physical properties, a large pixel size can be used, greatly reducing inspection times.

Because FEOL floating gate word line structures on flash memory products are similar to µLoop test structures, that methodology can be applied without having to manufacture special test structures. Using the method on product wafers enabled Fab 25 to detect killer defects in approximately an hour per wafer, increasing throughput dramatically. That accomplishment greatly accelerated the learning cycle, allowing Spansion to trace the sources of the defects quickly and alter the process to optimize sort yields.

Electrical Defect Monitoring Method

The µLoop electrical defect monitoring method uses a specialized test structure together with an e-beam inspection system. The typical test structure (figure 1) shows a comb pattern with a set of lines tied together and grounded, along with an alternate set of lines that are floating and discrete. Electrical defects that occur in comb structures such as opens or shorts create a strong electrical signal during e-beam inspection. The defect monitoring method takes advantage

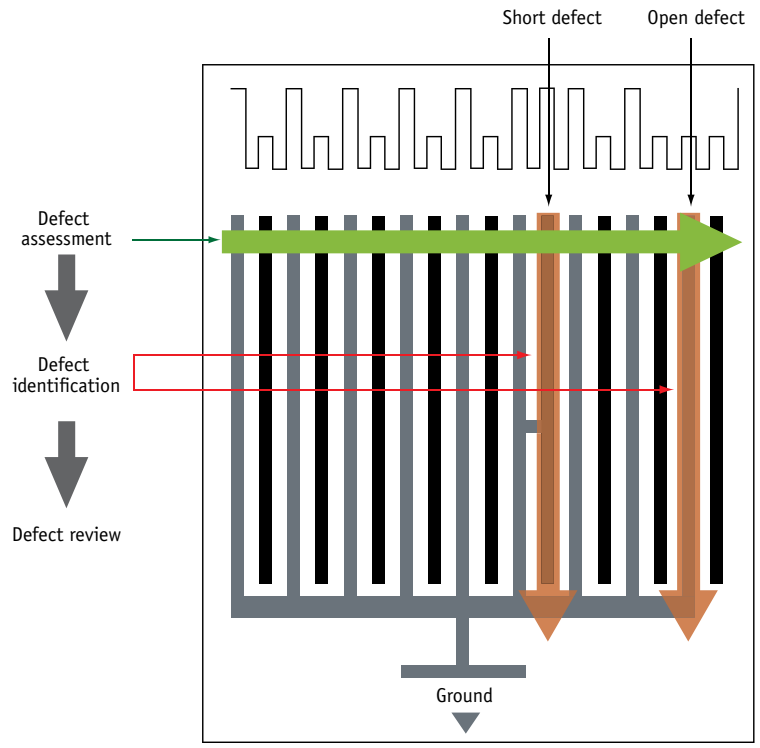

Figure 1: Principle behind the µLoop method. The diagram shows the comb-type structures and an electrical short and open.*

of that signal so that only a portion of the structure must be inspected to locate defects.

The method performs two separate scans to fully characterize defect density. The first scan, called the assess scan, is used to determine the locations of electrical defects in the x dimension—in other words, the lines on which the defects lie. The assess scan can also be used to estimate electrical defect density. The second scan is used to locate the defects in the y dimension. Called the identification (ID) scan, it is made at right angles to the first scan along each line identified as having a defect. After the defect coordinates have been determined, e-beam inspection is used to generate detailed images of the defects for classification and prioritization. At Fab 25, an eS31™ e-beam tool from KLA-Tencor was used.

Since Spansion's floating gate word line structures have layouts that mimic standard µLoop test structures, the use of the electrical defect monitoring method on product wafers followed the same inspection routine as that performed on test structures. As shown in figure 2, an assess scan (at left) was performed followed by an ID scan (right), which detected killer electrical defects only.

Applying the Defect Monitoring Method to a Co_xSi_y Excursion

During routine electrical testing of 110nm NOR flash product, Fab 25 discovered a yield excursion in the Co_xSi_y layer of the floating gate word line structures. A scanning electron microscope image of the defect is shown in figure 3. The culprit, illustrated in the schematic cross section in figure 4, proved to be a Co_xSi_y fiber defect that bridged the Co_xSi_y word lines and caused a direct electrical short. The defect was difficult to detect using optical inspectors for two reasons: First, its composition and, therefore, its optical properties are very similar to those of the Co_xSi_y lines on which it lies, and second, it had a diameter of <20nm. While fab personnel were able to

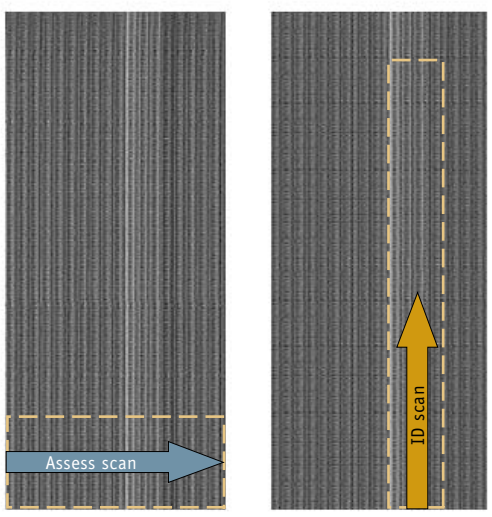

Figure 2: Two types of scans performed in the µLoop method: Co_xSi_y assess scan (left) and Co_xSi_y ID scan (right).

*Graphic courtesy of A Shimada, "Application of µLoop Method to Killer Defect Detection and Inline Monitoring for FEOL Process of 90nm-Node Logic Device," IEEE/SEMI Advanced Semiconductor Manufacturing Conference and Workshop, Boston, May 4–6, 2004.

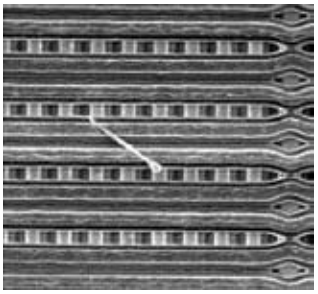

Figure 3: Top down SEM image of a killer Co_xSi_y fiber defect on top of a Co_xSi_y word line and active floating gate memory device features.

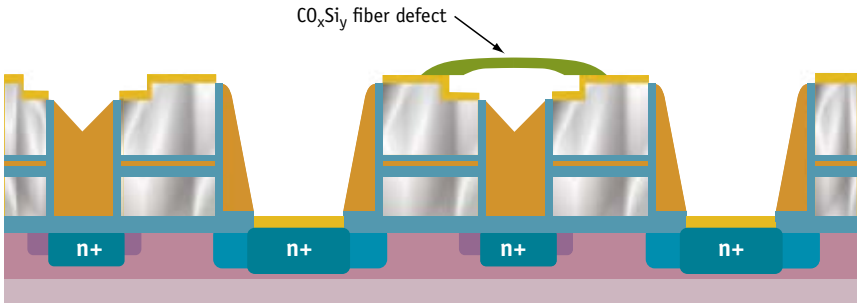

Figure 4: Cross section of typical floating gate flash memory FEOL word line structures and a Co_xSi_y fiber killer defect bridging the Co_xSi_y word lines. This defect would cause a direct electrical short.

detect the defects using traditional e-beam inspection with a pixel size of 100nm, that method proved time-consuming and detected many artifacts associated with the shorting effects of the Co_xSi_y fiber defect.

In order to reduce the inspection time dramatically and focus on the killer Co_xSi_y fiber defects, a joint task force of Spansion and KLA-Tencor engineers was formed. The breakthrough came when the engineers recognized that the word line structures have a similar geometry to the alternating pattern of grounded and floating lines that comprise µLoop test structures. Hence, they decided to perform an experiment in which µLoop methodology was applied to the Co_xSi_y layer on product wafers.

The electrical defect monitoring method can differentiate between DOIs—in this case, Co_xSi_y fiber defects—and artifacts caused by associated shorting. That ability resulted in the elimination of non-DOI defects. In contrast, a standard e-beam inspection tool captured 297 artifacts. By ignoring the non-DOI defects, the new method realized substantial inspection time and tool throughput improvements.

Inspection times were reduced by more than 50%, while tool throughput increased by 71%.

Based on those results, Spansion became interested in deploying µLoop on the production floor. To that end, the team began testing the method on the Co_xSi_y layer of multiple production wafers. The application was set up in the same manner as a µLoop test chip, and initial inspection results were fast and accurate.

Figures 5a and 5b compare wafer maps of the Co_xSi_y process layer generated during standard e-beam inspection and µLoop inspection, respectively. The standard e-beam scan captured 304 total clustered and non-clustered defects, only seven of which were identified as Co_xSi_y fibers, while the µLoop scan captured only seven defects, all of which were found to be Co_xSi_y fiber defects. Since the electrical defect monitoring method had a similar capture rate for fiber defects as the standard e-beam method, also without nuisance defects, split lots were run using µLoop inspections to identify and resolve the root cause of the killer defect.

Root-Cause Identification and Implementation of Process Change

Employing the defect monitoring method on multiple process split lots, the team conducted several short learning cycles and quickly identified the root causes of the fiber defects. They determined that the interaction of three different process modules was responsible for the defects: shallow trench isolation, stacked gate mask, and poly 2 etch. The most manufacturable solution to the problem was to introduce a new middle-of-the-line (MOL) photoresist/masking process.

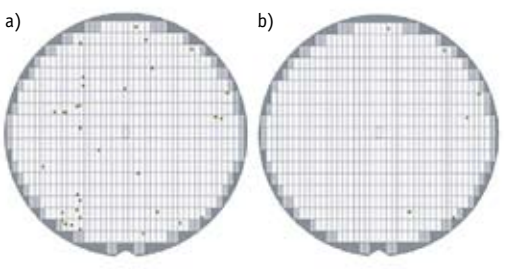

Figure 5: Defect inspection results from (a) standard e-beam inspection and (b) the µLoop method.

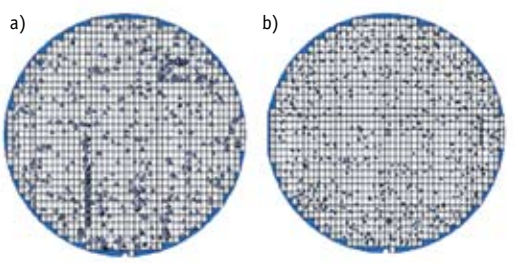

Figure 6: Overlay wafer maps of e-beam scans from the Co_xSi_y layer from wafers processed using (a) the standard photoresist process and (b) the new photoresist process.

Once again, e-beam inspection and the defect monitoring method were employed to collect inline defect data from the Co_xSi_y layer, with the goal of identifying the specific photoresist process change that eliminated the Co_xSi_y fiber defects. Figure 6 compares an overlay wafer map from the original process with a map from the process with the new MOL photoresist/masking step. The fiber defects from the original process are located in the vertical clustered streak on the lower left side of the map in figure 6a. In contrast, the map from the wafers processed using the new MOL photoresist process (figure 6b) is free of the streak, indicating that fiber defects are not present.

Further evidence that the new photoresist/masking process generates fewer defects than the standard process is presented in figure 7. Figure 7a compares the total number of defective die resulting from defects on the Co_xSi_y layer for the standard versus the new process, while Figure 7b compares the end-of-line sort 0 yield bin correlated to the Co_xSi_y defects for the old versus the new process. Both the defectivity data and the sort 0 yield loss data demonstrate that the new MOL photoresist/masking process eliminates the Co_xSi_y fiber defects.

Conclusion

Floating gate word line structures on flash memory products have layouts that are uniquely suited to being tested using µLoop technology and e-beam inspection. Spansion's Fab 25 used this approach to detect small physical defects that were causing a yield excursion in the cobalt silicide layer.

In addition to detecting the Co_xSi_y fiber defects, the electrical defect monitoring method was used to conduct short-loop experiments to determine the root causes of the defect and to qualify a new MOL photoresist/masking process to correct the problem. The µLoop method was shown to eliminate artifacts, improving inspection times by more than 50% and throughput by more than 70%. Since this work was completed, the method has been employed in the fabrication of Spansion's 90nm MirrorBit™ flash products.

Acknowledgments

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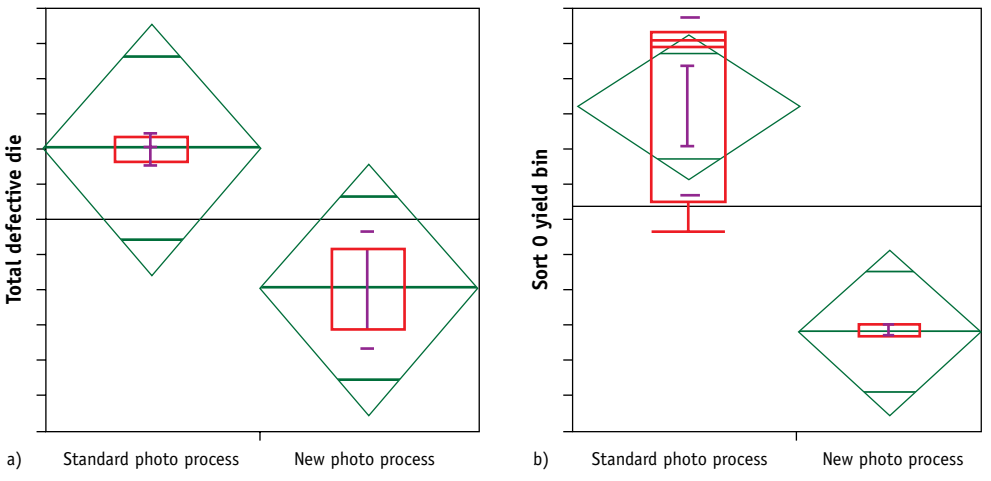

Figure 7: Correlation of e-beam inline defect scans to end-of-line sort yield losses: (a) shows inline defectivity resulting from the standard versus the new photoresist process, while (b) shows sort 0 yield bin data for the standard versus the new photoresist process.