In the Thick of Multilayer ARCs

Leonard J. Olmer, Robert W. Bradshaw, and Robert Morgan Young, Agere Systems
Arun Srivatsa, KLA-Tencor Corporation

A robust multilayer DARC measurement recipe can be developed to routinely monitor DARC thickness, index and extinction coefficient on product wafers. The recipe can also provide the underlying hard mask and polysilicon thickness, resulting in a simultaneous measurement of 10 parameters. The method increases tool availability, cuts down on process monitor wafers, and reduces gas use and operator costs.

Introduction

Dielectric antireflective coating (DARC) structures based on three in situ-deposited layers of silicon oxynitride (triple-ARC structure) with different thicknesses and compositions are widely used for lithography at Agere Systems.[1] The DARC's unique design permits wide process window latitude and provides applicability to different underlying "product" structures. However, for process monitoring, the simultaneous measurement of the triple-ARC SiON stack on an underlying product structure poses a challenge. For some time, the monitoring scheme was based on measurements of the thickness and optical properties of each SiON layer deposited on separate silicon control wafers.

A robust monitoring scheme was developed for the triple-ARC structure directly on product wafers using spectroscopic ellipsometry (SE). Experimentation was done in which process conditions were varied to establish correlations between the measured parameters for the triple-ARC structure on product, triple-ARC structure on silicon, and each of the single-layer SiON films on silicon. Following development, this monitoring scheme was implemented in production and is used at a number of Agere facilities to routinely monitor the triple-ARC structure on product wafers. The triple-ARC structure is greatly simplified by a single-pass measurement on product wafers that simultaneously monitors 10 parameters.

The manufacturing process for current semiconductor technologies requires a precise photo exposure process. The photoresist must be exposed for a specific amount of time at a specified location using a known light wavelength. When exposing photoresist, it is important that only the required areas be exposed. Any parameter change can result in distorted photo patterns that lead to device problems. The light used to expose the photoresist can be reflected from underlying structures, exposing areas where it is undesirable to do so. Anti-reflective films have been developed to address this issue and are deposited prior to the photo process to minimize reflections.

PECVD is the current method of choice for depositing these films because of its etch-selectivity to photoresist, low defect density, and low deposition temperature, which is required when depositing over interconnect such as aluminum. The PECVD method relies on the introduction of specific gaseous precursors, silane (SiH_4) and nitrous oxide (N_2O), into a PECVD chamber at very specific flow rates and deposition times to form SiON films. There are other factors involved with PECVD; however, many of these are tool-specific and

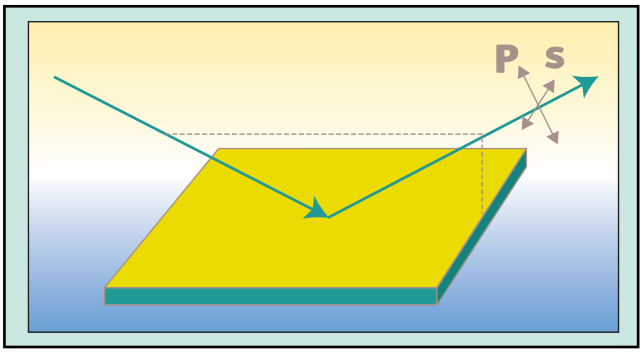

Figure 1. Schematic showing reflection of polarized light from a surface.

may vary between manufacturers and process requirements. Generally, a change in the ratio of the flow rates of SiH_4 to N_2O affects the stoichiometry of the deposited film. This, in turn, influences the film's refractive index (*n* and *k*) where *n* is the real portion of the refractive index and *k* is related to the extinction coefficient. Deposition time is another key process parameter that affects the resultant thickness *t* of the deposited film. Since *t*, *n* and *k* are key factors in the film's ability to reduce reflectance, these parameters must be monitored and controlled to assure antireflective film performance.

Single-layer ARC films, as typically used, work on the principle of phase-shift cancellation and absorbance to eliminate reflections. Thus, ARC film properties and resist thickness must be carefully controlled. The uniqueness of Agere's triple-ARC process is the use of multiple ARC layers deposited sequentially to produce a triple-ARC stack that completely absorbs the reflected light during the photo process. This technique is more manufacturable than the single-ARC process because *n*, *k* and *t* do not have to be as tightly controlled.

In the manufacturing environment it is still necessary to measure the DARC optical properties. And it is better yet to measure directly on product wafers rather than on silicon control wafers. Measuring each layer's optical properties in the triple-layer stack deposited over underlying hard mask and polysilicon posed a problem. The benefit is the elimination of silicon control wafers and increased use of the plasma deposition tool to run product, which results in reduced cost.

Test matrix rationale

The goal was to implement the monitoring of the triple-ARC process directly on product. The intent was to produce DARC films with a predetermined range of thickness and refractive indices, which were deposited as individual layers along with correlating composite three-layer stacks. In theory, the measured parameters obtained from the single-layer DARC films on silicon should agree with those obtained from the same stacked film on silicon or on product.

The parameters measured for all of the films were *t*, *n* and *k* at 365 nm, the wavelength used during photo exposure. Due to the small difference in the *n* value between each film, the top and middle layers were combined for the stack measurements. In some instances, this small difference in the refractive index made it difficult to locate the interface between each layer. Therefore, the reported thickness is the sum of the top layer thickness and the middle layer thickness. The reported refractive index at 365 nm is the average value obtained from the top and middle layers. This should not affect the usefulness of the DARC measurement recipes since the measured parameters will still yield values that indicate an out-of-tolerance mass flow controller (MFC) or incorrect deposition time, if they occur.

A designed experiment having six factors was performed varying N_2O and SiH_4 ±10%, about the nominal values for each DARC layer. The deposition time for the top-, middle- and bottom-layer DARCs and hard mask was also varied ±1 sec. The intent was to produce DARC films that would be identical, with the exception that some were in a composite three-layer stack, and others were individual films on silicon.

DARC film measurement

Spectroscopic ellipsometry (SE) was used to measure the *t*, *n* and *k* of the DARC films.[2-4] This optical technique

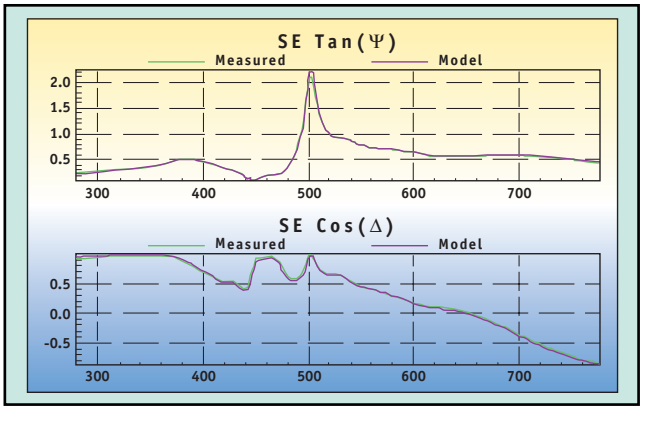

Figure 2. Tan(C) and cos(D) spectra from a DARC film stack on product. The measured spectra are plotted along with the results from the theoretical model.

is ideal for a production environment because it does not contact the wafer surface, is relatively quick and is capable of performing measurements on a variety of film stacks.

SE is based on the measurement of optical properties through analysis of polarized light reflected from the sample surface. The rotating polarizer version of this technique is used in KLA-Tencor systems, where the polarization state of the incident light is continuously varied and the detector measures the integrated intensity of the reflected polarized light at each wavelength across 1024 wavelengths of a broadband visible-UV spectrum. A broadband light source and a diffractor is used to separate the wavelengths of the light incident on the pixels forming the detector array. The integrated intensities of the polarized light can be used to compute standard ellipsometry parameters tan(C) and cos(D) at each of the 1024 wavelengths. These quantities are related to the two components R_p and R_s of the reflected polarized light, by the equation:

$$\tan(\Psi)\exp(i\Delta) = \frac{R_p}{R_s} \qquad (1)$$

where R_p is the component of polarization parallel to the plane of the incident and reflected beams, Rs is the component perpendicular to that plane as shown in Figure 1. It can be inferred from the above equation that tan(C) is the ratio of the $_{p-}$ and $_{s-}$ component intensities and cos(D) is the real part of the complex quantity exp(iD).

Theoretical spectra can be generated based on material models defining the substrate and film stack. A mathematical regression analysis is performed between the measured tan(C)-cos(D) spectra and theoretical computation. The theoretical spectra include optical dispersion models (RI as a function of wavelength) and thickness data for the film (or film stack) and the substrate. For accurate and repeatable results, it is critical to have a robust mathematical model of the optical dispersion. To solve for the parameters in the dispersion model and the film thickness (*t*), a regression analysis is performed so that the difference between the calculated and measured tan(C)-cos(D) spectra is minimized.

Recipe development for measurement

The main objective during the recipe development for the SE measurements was to maximize the amount of useful information that could be obtained by analysis. As stated earlier, key parameters measured for the

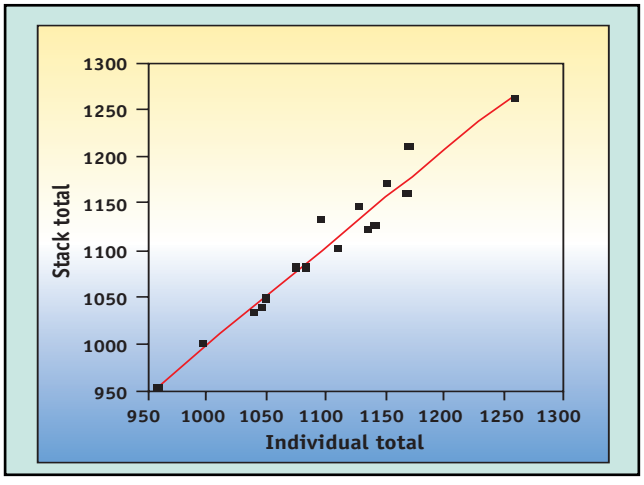

Figure 3. Correlation of total DARC thickness to the sum of the individual DARC thickness over silicon.

DARC films were *t*, *n* and *k* at 365 nm. In addition, for the DARC measurement on product, two of the layers beneath the DARC films were also measured. The thickness of the hard mask layer beneath the DARC films was measured, as well as *t*, *n* and *k* of the polysilicon beneath the hard mask. A total of 10 parameters (four thickness values and three sets of indices [*n* and *k*]) were simultaneously measured for the DARC film stack on product. An example of the spectral fit between the theory and model for a product stack measured in the DOE is shown in Figure 2.

Single-layer and stack data on silicon

Figure 3 displays the total stack thickness obtained from the sum of each of the single layers on silicon recipe,

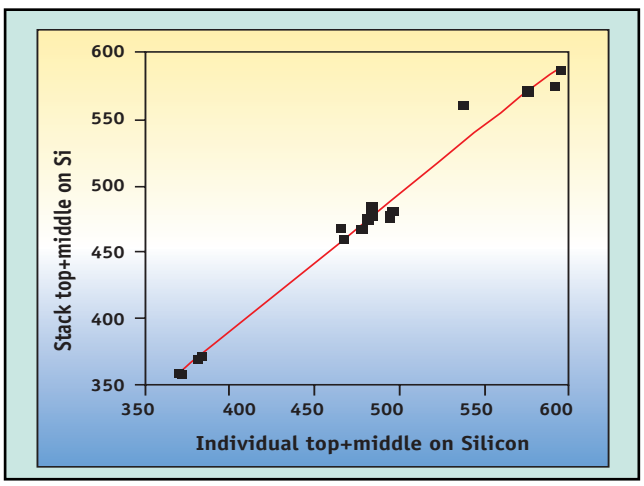

Figure 4. Correlation of top- and middle-layer DARC thickness; individual versus stack measurement.

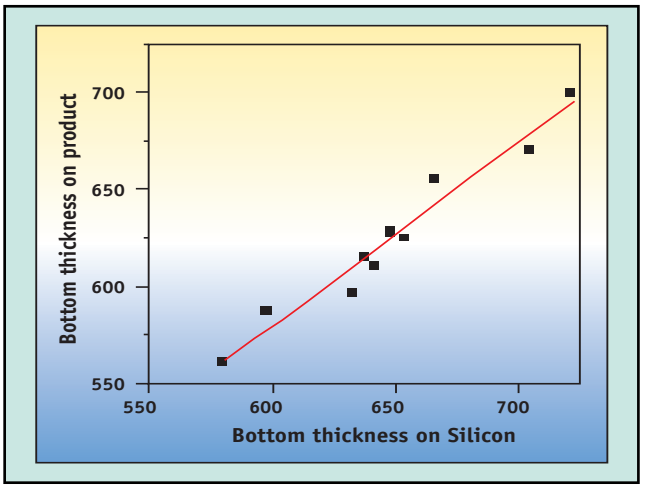

Figure 5. Correlation of DARC bottom thickness on silicon to bottom thickness on product.

compared with the thickness obtained using the DARC stack-on-silicon recipe. The red line is the best-fit straight line through the data. The root mean square (RMS) error from the best-fit straight line is ±6.4 Å. The tolerance for each layer in the three-layer stack is ±100 Å.

The sum of the measured thickness of the top- and middle-layer DARC film obtained from the single layer on silicon recipe is compared with the thickness values obtained using the DARC stack-on silicon recipe in Figure 4. The red line is the best-fit straight line through the data. The RMS error from the best-fit straight line is ±10.0 Å. The tolerance for each layer in the stack is ±100 Å.

Stack data on silicon and product

Figure 5 displays the measured thickness for the bottom-layer DARC film obtained from the DARC stack on silicon recipe compared with the thickness values obtained using the DARC stack on product recipe. The red line is the best-fit straight line through the data. The RMS error from the best-fit straight line is ±9.5 Å. The bottom thickness on silicon measured; 23 Å thicker than the bottom thickness on product. This can be seen by the X intercept of the red line on the X axis. The magnitude of this difference is not large enough to prevent the use of this model as a production inline monitor. Further, this observation was found to be consistent with results from limited TEM analysis. Tolerance for the bottom layer *t* is ±100 Å.

Figure 6 displays the sum of the measured thickness of the top- and middle-layer DARC film obtained from the DARC stack on silicon recipe compared with the thickness values obtained using the DARC stack-on-product recipe. The red line is the best-fit straight line through the data. The RMS error from the best-fit straight line is ±10.7 Å. The tolerance for each layer in the stack is ±100 Å.

Figure 7 displays the total stack thickness obtained from the DARC stack on silicon recipe compared with the thickness values obtained using the DARC stack on product recipe. The red line is the best-fit straight line through the data. The RMS error is ±11.2 Å. The tolerance for each layer in the three-layer stack is ±100 Å.

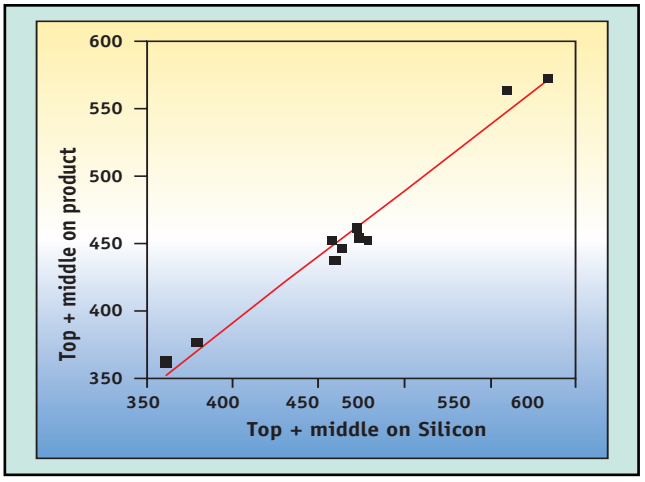

Figure 6. Correlation of DARC top and middle thickness on silicon to top and middle thickness on product.

Production data

The recipes were implemented into production and the collected data is running at expected levels with excellent stability. The on-product SPC chart shown in Figure 8 is an example of the data collection now in place for product measurements. Notice that the total stack thickness measures; 20 Å low, which is consistent with the 23 Å measurement difference noted in Figure 5. The total stack thickness information is obviously very useful for detecting a problem quickly.

The agreement between the single layer on silicon to the DARC stack-on-product measurement results gives an indication of what kind of agreement can be expected in a production environment. Figure 9 gives the (*n*) results plotted on a scale that encompasses the ±0.15 tolerance for this measurement. It is well within the ±0.15 tolerance for the measurement.

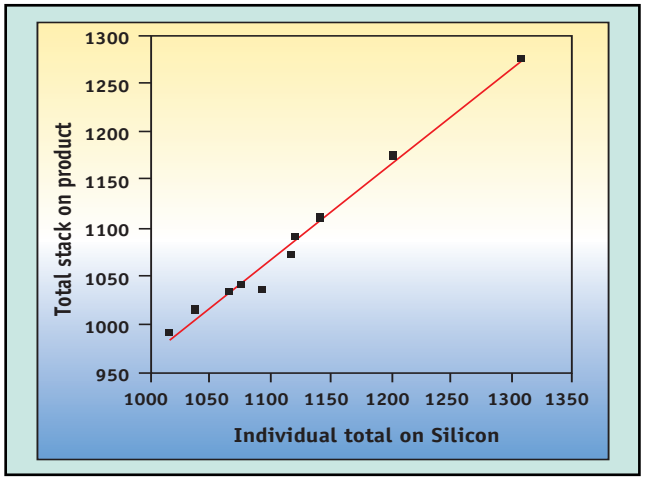

Figure 7. Correlation of DARC total thickness on silicon to total thickness on product.

The stack measurement model on product has also allowed the measurement of other layers from other deposition process tools. We routinely measure the hard mask and polysilicon film thickness on product. A comparison of the hard mask thickness measurement on product before the DARC film stack deposition and following the DARC film stack deposition is shown in Figure 10. As seen, the two measurements are statistically equivalent.

It is possible to develop a robust multilayer DARC measurement recipe that can be used to routinely monitor DARC thickness, index and extinction coefficient on product wafers. Measurement capability has been demonstrated by the agreement between the single-layer DARC, three-layer DARC on silicon and three-layer DARC on product results. In addition, the on-product recipe can also provide the underlying hard mask and

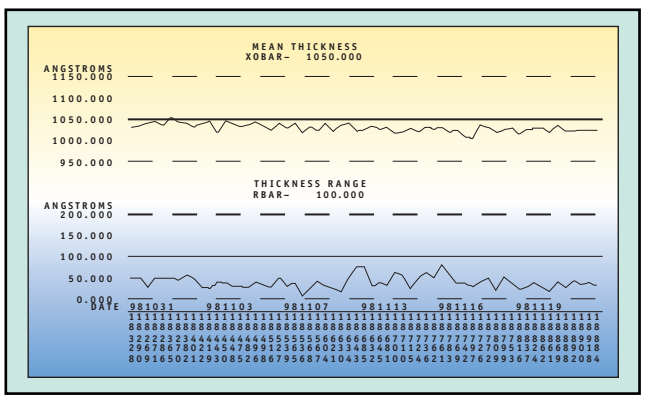

Figure 8. Total DARC stack thickness as measured on product.

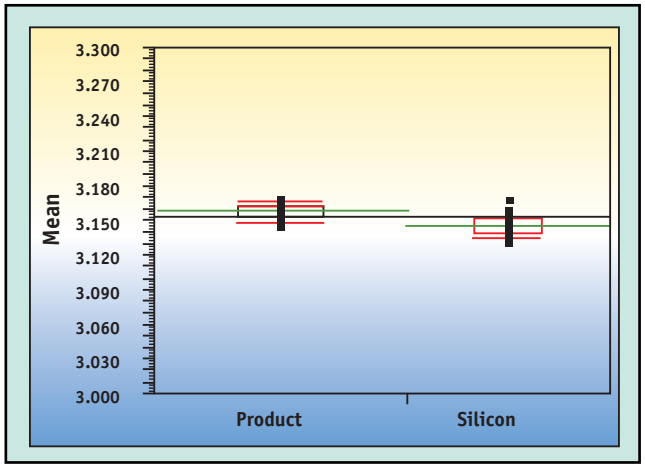

Figure 9. Bottom layer *n* at 365 nm for DARC stack on product and single-layer DARC on silicon.

polysilicon thickness, resulting in a simultaneous measurement of 10 parameters. Cost savings result from increased tool availability, a 75% reduction in process monitor wafers, and reduced overhead expenses such as gas use and operator costs. The total cost savings add up to; $200,000 per year, per process tool. Additionally, there is great benefit to being able to measure directly on product wafers to detect process drifts using a higher sampling frequency.

Acknowledgements

The authors wish to thank Tod Robinson and Bill Henderson of KLA-Tencor and Kristen Waxman for their help in this work. This article was originally published in Semiconductor International (online), July 2002, http://www.e-insite.net.

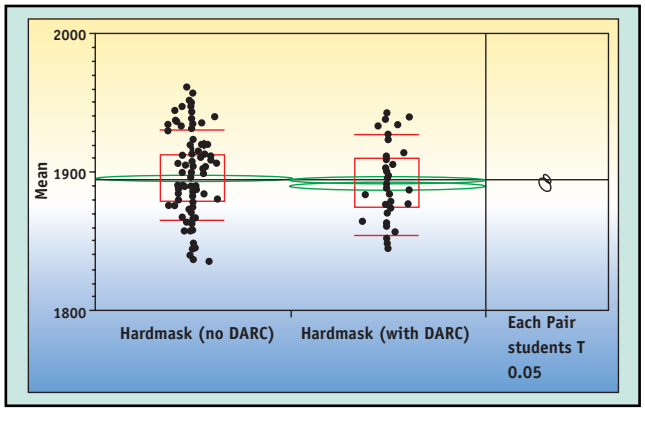

Figure 10. Comparison of hard mask thickness measurements on product before and after the deposition of the DARC film stack.

References

1. R.A. Cirelli, et al, "A Multilayer Inorganic Antireflective System for Use in 248 nm Deep Ultra-violet Lithography," *Journal of Vacuum Science and Technology B*, Vol. 14, No. 6, 1996, p. 4229.
2. K. Vedam, "Spectroscopic Ellipsometry: A Historical Overview," *Thin Solid Films*, Vol. 313-314, No. 1-2, 1998, p. 1.
3. R.M.A. Azzam and N.M. Bashara, *Ellipsometry and Polarized Light*, North Holland, Amsterdam, 1997.
4. A.R. Srivatsa and C. Ygartua, *Optical Metrology*, Ghanim Al-Jumaily, Ed., SPIE Optical Engineering Press, 1999, p. 61.

KLA-Tencor Trade Show Calendar

March 11-13	SEMICON China, Shanghai, China
March 24-26	IC China, Shanghai, China
April 1-3	SEMICON Europa, Munich, Germany
April 10-12	DISKCON Japan, Tokyo, Japan
April 16-18	Photomask Japan, Yokohama, Japan
July 14-16	SEMICON West, San Francisco, California
July 16-18	SEMICON West, San Jose, California