Shining Spotlight on SOI Wafers

A New Approach to Detecting Subtle Etch Variations

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In advanced fabs, silicon-on-insulator (SOI) wafers are becoming increasingly popular for their low power consumption and high processing speed, as compared with conventional wafers. This growth has generated a need to implement electron-beam inspection (EBI) of SOI wafers with a new approach. While EBI has proven its effectiveness on bulk material, the same needed to be demonstrated with SOI wafers. IBM's 300 mm production fab applied EBI to inspect its SOI wafers for Reactive Ion Etch (RIE) process variation on tungsten local interconnect levels. Through this process, IBM was able to demonstrate that its eS31 system was able to find subtle etch variances.

Introduction

Electron-beam inspection (EBI), through the use of voltage contrast, is used extensively throughout the industry to identify inline electrical failures. In fact, EBI has become a widely accepted addition to semiconductor fabrication yield strategies. Like other inspection strategies, EBI needs to be sensitive to critical defects of interest (DOI) and also be stable. It also should provide minimum charging and contain low amounts of nuisance. However, it is becoming apparent that in order to meet these objectives for silicon-on-insulator (SOI) technology, a new approach to EBI is required.

Unlike conventional wafers, the SOI wafer contains three layers. The first is a single-crystal layer of silicon with a thickness of 1 mm or less. The other two consist of a base silicon substrate and a thin insulator that electrically insulates the single-crystal layer from the substrate. The thin insulator prevents the parasitic or incidental capacity usually induced between a device and the substrate for conventional wafers. The result is lower power consumption and higher processing speeds. SOI is becoming more popular in advanced semiconductor fabs for this reason.

EBI methodologies and different materials

Conventional substrate

EBI has been proven effective on bulk material, especially for the inspection of tungsten (W) plug integrity.The voltage contrast signal is also easily reproducible with an ion beam, making the affected contact easy to redetect in cross section. Figure 1 shows a typical open W contact after fill and planarization that was detected through voltage contrast inspection.

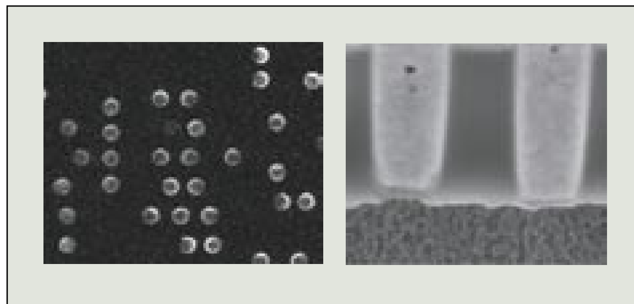

Figure 1. Voltage contrast (left) of W contact indicating underetch (right) on conventional wafer.

SOI substrate

The concept of SOI intuitively suggests that the insulator box would prevent a direct path to a grounded state and, therefore, prevent the generation of strong voltage contrast for EBI. Empirically, however, voltage contrast can be obtained on SOI wafers as seen in Figure 2, and is most likely the result of capacitance variations. Additionally, the top thin silicon layer may serve as an electron sink. Here we see voltage contrast W contact connected to PFET indicating an open.

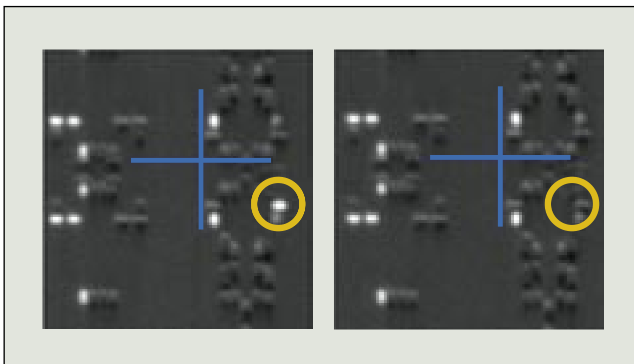

Figure 2. Voltage contrast of W contact indicating underetch on SOI wafer.

SOI substrate and W local interconnect

Some difficulty arises when inspecting for voltage contrast on a W contact layer where the W structures act as local interconnects. These short metal lines may bridge several devices as well as the shallow trench isolation (STI). In this situation, the capacitance variation that causes voltage contrast on a filled W structure may become redundant and no signal is observed. However, if the inspection occurs prior to metallization fill, an underetch signal can be seen. Figure 3 illustrates the EBI image of unfilled W local interconnects just after RIE etch. It is important to note that EBI at this layer requires charging effects to be minimized. A capability on the KLA-Tencor eS3X was used to predose the wafer with electrons, which reduced localized charge non-uniformity.

Within one line structure, the gray scale can alternate between being completely black and being bright white. This is the result of differing secondary yield coefficients for the two materials located at the prior level. The black regions represent regions of STI. The bright regions represent diffusion or polysilicon regions that are covered with silicide. Figure 4 shows a normally dark region now appearing bright.

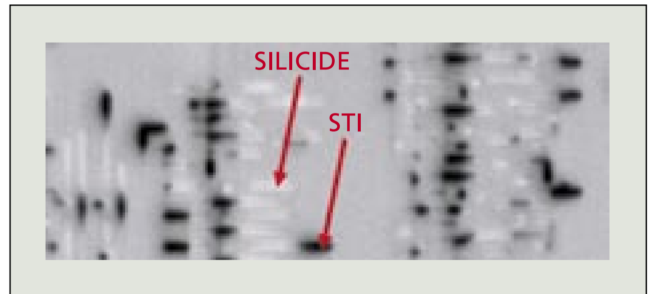

Figure 3. Material contrast seen through an etched local interconnect level prior to W fill.

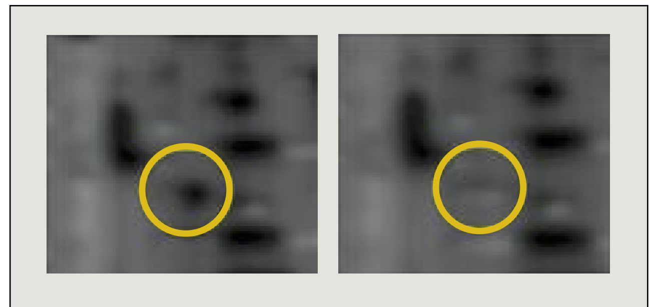

Figure 4. Material contrast seen through an etched local interconnect level prior to W fill.

The defect from Figure 4 and others in the vicinity are believed to be the results of subtle barrier nitride underetch. The TEM cross section image of this area can be seen in Figure 5.

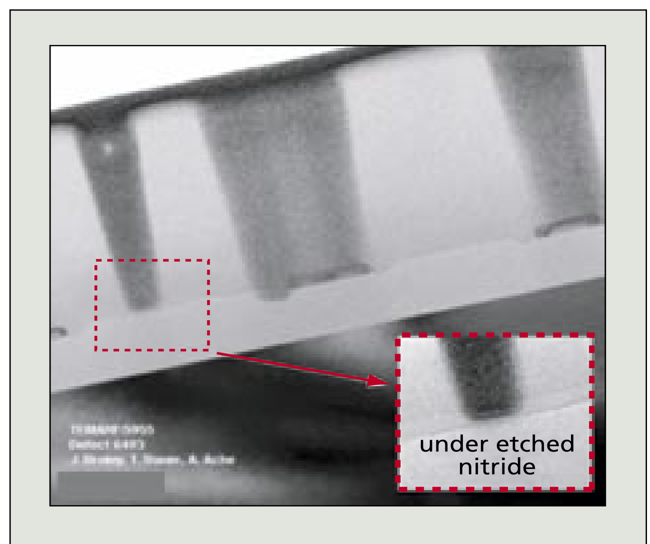

Figure 5. Material contrast seen through an etched local interconnect level prior to W fill.

SOI vs. conventional substrates

The conditions needed to generate an optimum EBI signal for detection of open W contacts is presented in Table I. The table shows the conditions for both conventional and SOI wafers for pre- and post-W metallization.

	e-Beam Landing Energy (eV)	e-Beam Current (nA)
Conventional Wafer Pre-W Fill	750 - 1000	75
SOI Wafer Pre-W Fill	500	25 - 75
Conventional Wafer Post-W Fill	1000 - 1500	125
SOI Wafer Post-W Fill	500 - 750	75

Table I. E-beam conditions for conventional and SOI wafers.

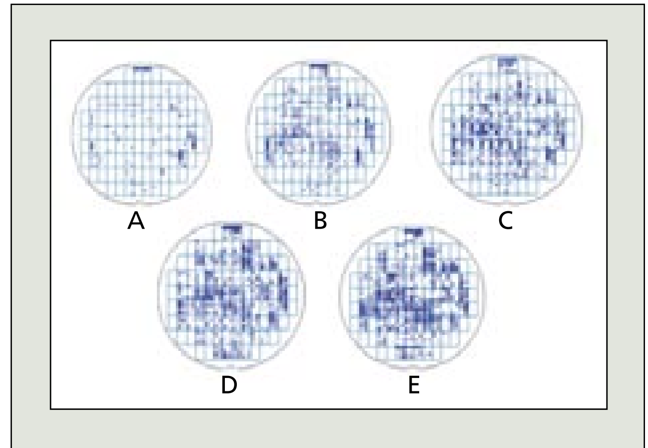

Figure 6. Material contrast seen through an etched local interconnect level prior to W fill.

Case study: Seeking subtle underetch on W local interconnect

Parameters

A case study was conducted at IBM's 300-mm production facility in search of subtle underetch on W local interconnect structures. The goal of the experiment was to determine the optimum process conditions for achieving proper selective-etch conditions. A group of 10 wafers was split into five distinct processing conditions for inspection on the KLA-Tencor eS31.

A high extraction field was used on the wafer in order to maximize the signal. In addition, the wafer was preconditioned with a negative charge prior to the inspection. The inspection pixel size was done at .10 µm in a die-to-die comparison.

Results

The overlay defect wafer maps can be seen in Figure 6. There does seem to be some degree of regionality to the defects, even across the various process conditions.

Figure 7 shows the results, and indicates that process split A is the best choice for the RIE process condition.

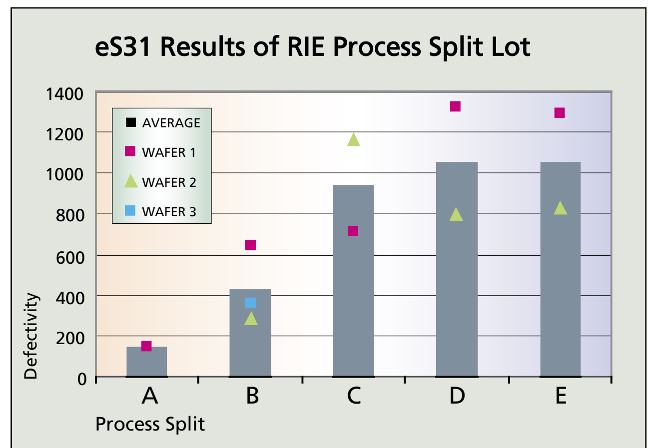

Figure 7. Material contrast seen through an etched local interconnect level prior to W fill.

Conclusion

Inspection for voltage contrast events on SOI wafers requires additional attention compared to the conventional wafer counterpart. However, this study has proven that electrical defectivity can be identified through e-beam inspection and voltage contrast is still a viable method. Care must be taken to establish proper beam conditions that do not induce high levels of charging across SOI wafers.

This article is based on a paper that was originally presented at ASMC 2005.

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