The Future's All About Cost…

Many of us have pondered about the end of the classical Moore's Law, the prediction that integrated circuit functions would double in density every 18 months. For more than 20 years, Moore's prediction has relied primarily on device scaling. That era is coming to an end, partly due to the failure of the 157 nm and EUV lithography roadmaps and partly due to more fundamental limitations such as power dissipation in small devices. Ultimately, it all boils down to cost. If new materials, device architectures, and means of production are significantly more costly or less efficient, they will not be used; and older technologies will be extended. Currently, the semiconductor industry is at such a crossroad.

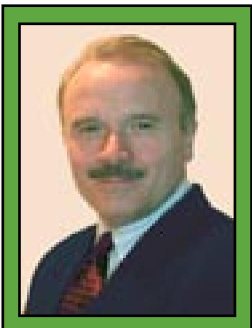
Most semiconductor manufacturers expect 193 nm immersion lithography to remain the dominant patterning technology through the 32 nm technology node. Even now, the interaction of more complex designs with shrinking process windows is having an impact on parametric yield in early production. The semiconductor industry is addressing this problem using design for manufacturability (DFM) and advanced process control (APC) strategies. The exact definition of DFM and APC can vary significantly with context, particularly when comparing foundry, logic, and memory products. In each case, however, the primary goal of DFM is to enlarge the process yield window, and the primary goal of APC is to keep the process in that yield window.

Enabling DFM and APC strategies with metrology will require significant innovation. As a minimum, DFM will require feeding forward design intent, simulator output, layout clips, and DRC hot spots to expedite setup of measurement tools. Current design-rule-check (DRC) and aerial image modeling at best focus and exposure conditions is increasingly unreliable. In the future, process window-aware approaches will require powerful full-chip simulators that can accurately predict and measure developed patterns in resist, along with a super-computing environment that can produce results in an acceptable timeframe. To control development costs, the conversion of data to information, knowledge, and decisions will be taken as far upstream as possible.

On the process control side, implementing an APC strategy requires feeding forward both process context and measurement data. In the future, we know that process context and measurement data must increase dramatically to support multi-variate control at the lot, wafer, field, die, and intra-die levels. In addition, yield and performance losses are often caused by integration issues or combinations of profile, shape, roughness, thickness, and pattern placement errors. For these applications, additional measurement types are required, creating a need to decrease the cost and increase the yield-relevance of each measurement.

Despite the cost, DFM and APC are growth areas for the semiconductor industry. The economic trade-off between yield loss and process control is driving an increase in capital and service expenditure to support more sophisticated DFM and APC strategies. The case for linking design, layout, mask, and wafer processes with metrology is compelling. Greater complexity is offset by the advantage of greater access to adjustment; an array of strategies generates higher return than just one.

That brings us back to Moore's Law. The extension of Moore's Law can no longer rely on scaling alone. Progress may depend more on innovation in materials, nanotechnology, architecture, and packaging. For example, a number of microprocessor manufacturers are introducing multi-core processors that promise increased speed and functionality with lower power dissipation. Clearly, whether the market is my teenage son, who owns every imaginable video game, or a global economy that hungers for productivity gains, there will always be customers for the capability that Moore's Law can deliver. In fact, a less than prophetic engineer once told me that a 20-MHz processor was more than adequate for desktop computing and that no one would ever need an upgrade. I replied that human eye-motor response is roughly 250 milliseconds and, ideally, results should be provided within this timeframe. I'm still waiting...



Dr. Kevin M. Monahan
Parametric Solutions Group
KLA-Tencor Corporation

Yield Management SOLUTIONS

EDITOR-IN-CHIEF
Uma Subramaniam

SENIOR EDITOR
Christine Young

CONTRIBUTING EDITORS
David Moreno
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Siiri Hage

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DESIGN CONSULTANTS
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CIRCULATION EDITOR
Nancy Williams

KLA-Tencor Worldwide

CORPORATE HEADQUARTERS
KLA-Tencor Corporation
160 Rio Robles
San Jose, California 95134
408.875.3000

INTERNATIONAL OFFICES
KLA-Tencor France SARL
Evry Cedex, France
33 16 936 6969

KLA-Tencor GmbH
Munich, Germany
49 89 8902 170

KLA-Tencor (Israel) Corporation
Migdal Ha'Emek, Israel
972 6 6449449

KLA-Tencor Japan Ltd.
Yokohama, Japan
81 45 335 8200

KLA-Tencor Korea Inc.
Seoul, Korea
822 41 50552

KLA-Tencor (Malaysia) Sdn. Bhd.
Johor Bahru, Malaysia
607 557 1946

KLA-Tencor (Singapore) Pte. Ltd.
Singapore
65 6367 6788

KLA-Tencor Taiwan Branch
Hsinchu, Taiwan
886 3 552 6128

KLA-Tencor Limited
Wokingham, United Kingdom
44 118 936 5700