# Considering Overlay Metrology in the DFM Discussion

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*Overlay metrology has become a cornerstone requirement which enables modern lithographic patterning. The mantra of metrology engineers in the litho cell and tool vendors alike has traditionally been TMU — Total Measurement Uncertainty — a metric which combines all sources of metrology tool-related uncertainty. Although relentless TMU reduction is essential, it is certainly not a sufficient condition to meet the overlay control needs for the 32 nm node and below. Many other "on wafer" contributors must be factored into the uncertainty equation. A wider scope in the definition of the overlay metrology process is required, particularly one which views it as part of the greater IC manufacturing process. Current and emerging overlay metrology industry practices will be reviewed in light of the increasing complexity associated with the interactions between metrology tool, target design, and the sampling plan.*

## Introduction

TMU is a statistical concoction whose definition varies markedly over the globe[1-2], but is generally structured as a root sum squares of a combination of short-term precision, long-term precision, across wafer tool induced shift variation, and tool-to-tool matching. Interestingly, with respect to overlay metrology, the term TMU does not even appear in the 2004 ITRS roadmap, where reference is made to precision with the qualification that it includes tool-to-tool matching[3]. That is why the overlay metrology process should be viewed as part of the greater IC manufacturing process. This is illustrated schematically in Figure 1. In this article a definition of the meaning of Design for Manufacture (DFM) in the context of overlay metrology will be proposed. The design process will then be illustrated by two case studies which exemplify two of the steps in the process.

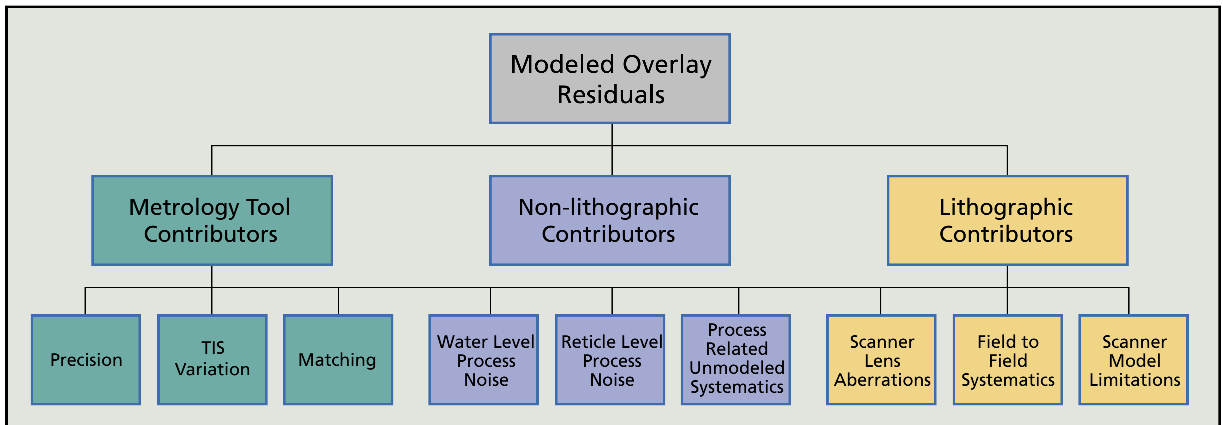


Figure 1. Schematic depiction of uncertainty contributors to overlay model residuals.

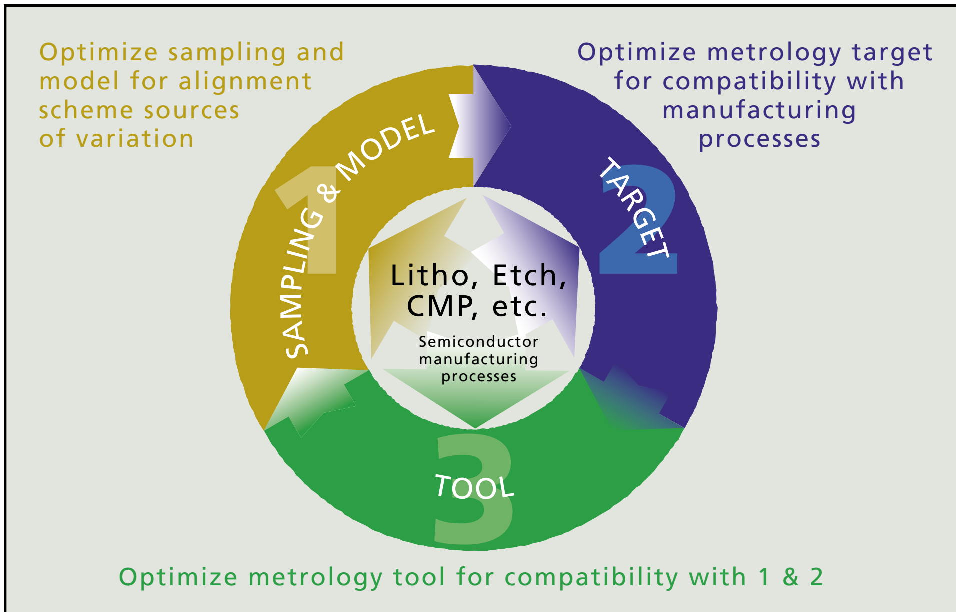


Figure 2. Schematic depiction of DFM methodology for overlay metrology, showing the three elements of sample and model, metrology target, and metrology tool. Semiconductor manufacturing processes are at the center, driving the requirements of all three elements.

### What is DFM for overlay metrology?

DFM in overlay metrology dictates recognition of the three elements in the metrology process: *sample plan/model, overlay target,* and *overlay tool.* Figure 1 is a graphical representation of these three overlay metrology system components and the dependencies between them. A DFM approach puts the semiconductor manufacturing process at the center, driving the requirements for each of the elements. Amongst the three elements exists a clear hierarchy within the triad, defining the sequence of optimization. The sample plan and the model must be a primary consideration in the overall system design, as this is driven directly by the overlay control error budget and the sources of variation characteristic of the alignment scheme in question. Next in the optimization sequence is the overlay mark design. This is impacted directly by the sample plan, e.g. target size requirements. Compatibility with the semiconductor manufacturing process, e.g. maintaining pattern density requirements for compatibility with CMP, is also a factor. The metrology tool is placed at the bottom of the hierarchy, since its design and performance parameters are derived by demanding compatibility with all of the above; for example: the ability to meet metrology uncertainty requirements on optimized metrology marks with throughput, which meets cost of ownership requirements driven by specific sample plans. This approach may seem obvious but has not necessarily been the case in the past. As will be demonstrated in the example below, significant opportunities exist to improve the DFM process on overlay metrology.

*Example 1 — Sampling and Model Optimization*

Modeling of overlay metrology data is performed routinely on data acquired on product wafers. This type of modeling serves two primary purposes, lot dispositioning and feedback of correctibles to the exposure tool.

Today, a frequently applied method of overlay modeling is the "double pass" method

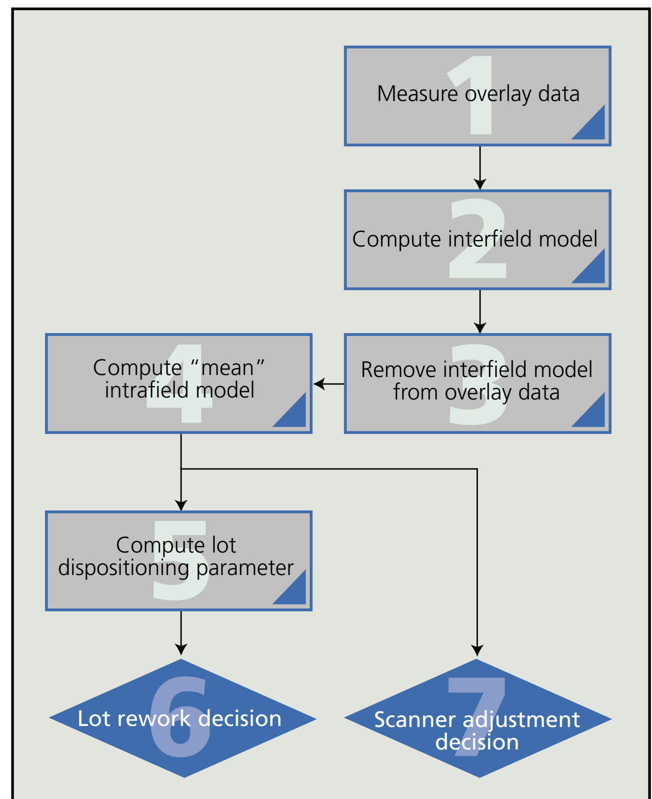


Figure 3. Typical overlay metrology modeling sequence, known as the double pass method enabling both lot rework and scanner adjustment decisions.

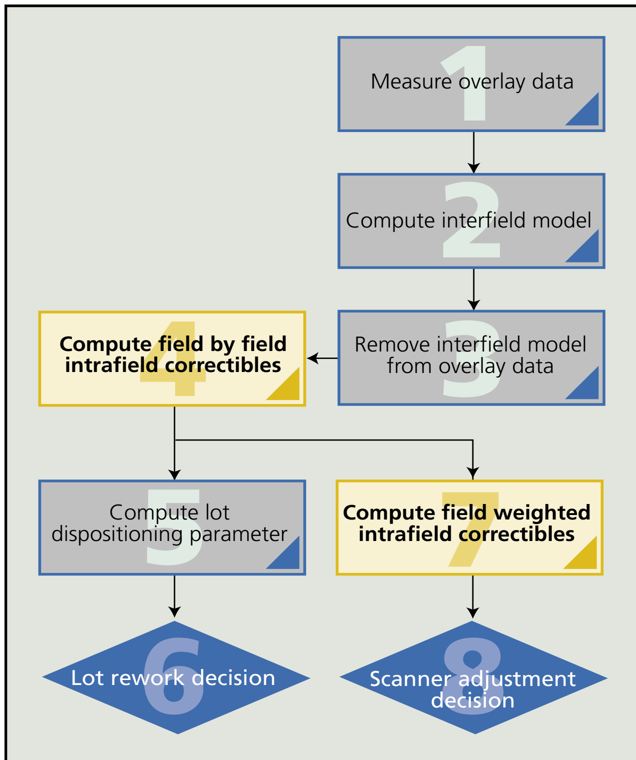


Figure 4. Modified overlay metrology modeling sequence, in which the mean intrafield model step is modified and additional weighting is enabled.

described in the flowchart, depicted in Figure 3. In this method it is assumed that the sources of overlay variation across the wafer may be divided into wafer level or "interfield" contributors and field level or "intrafield" contributors. In keeping with this assumption, under normal high-volume production circumstances, only two sets of correctibles, one linear in wafer coordinates and one linear in field coordinates, are fed back to the exposure tool's wafer and reticle stages, respectively.

These correctibles are also used for the purpose of computing a lot dispositioning parameter such as maximum predicted overlay (MPO), the second key decision driven by overlay metrology data. This procedure is diagrammed in Figure 3. Overlay metrology data may show significant field-to-field variation in the intrafield model terms[4]. As a result, the model residuals—that is, the differences between the measured overlay and that computed by the model at the same point—are often strongly influenced or even dominated by the field-to-field variation, since the standard model relies on "average" intrafield model terms.

This is a strong indication that an opportunity exists to improve lot dispositioning and correctibles accuracy. An alternative modeling sequence to that in Figure 3 is shown in Figure 4. In this case, intrafield correctibles are computed field by field prior to calculation of MPO or any other lot dispositioning parameter. Furthermore, the intrafield correctibles sent back to the scanner can now be determined in a more sophisticated fashion, which may give weight to or even ignore certain fields based on other criteria such as overlay target asymmetry, target noise, or even alignment data from the scanner. Alternatively, if the intrafield model is allowed to vary from field to field, then the impact of this field averaging on the model residuals can be quantified. Figure 5 shows the three sigma overlay model uncertainty at the field corners due only to the field-to-field intrafield correctibles variability. This calculation has been performed on overlay data from both production environments and R&D studies.

*Example 2 — Target Optimization*

Today, virtually all semiconductor manufacturers live with model residuals which are well beyond the level anticipated based on metrology tool or lithography process uncertainty contributors. Furthermore, some manufacturers are forced to add costly process steps because the metrology tool/target interaction is negatively impacted by CMP, deposition, or etch processes.

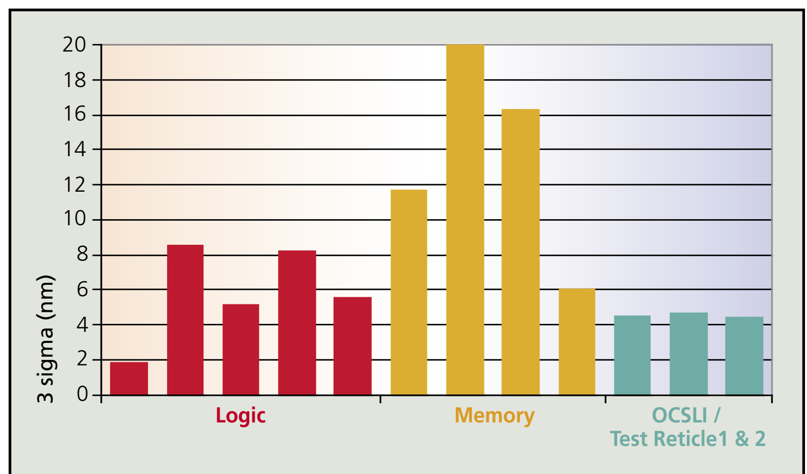


Figure 5. Three sigma overlay model uncertainty at the field corners due only to the field-to-field intrafield correctibles variability. Data from 130 and 90 nm processes in both production and R&D environments.

A number of advanced IC manufacturers are overcoming these challenges by adopting new practices including using AIM targets for improved process compatibility and stability. The AIM target, as opposed to the box-in-box target, is comprised of a grating structure[5], allowing it to meet pattern density requirements set down by other manufacturing steps such as CMP or etch. This has been characterized in a number of ways in previous publications[6-7].

Figure 6 shows box-in-box and AIM targets from different locations on wafers from a 130 nm FEOL flash memory process. The two examples of box targets on the left are from two different locations on the wafer. Strong variations in target asymmetry are observed in the images. On the right of the figure, images are shown of AIM targets printed adjacent to the box targets on the left. Although a contrast reversal is observed in the grating image between the two locations, image asymmetry is significantly reduced to enable a major improvement in metrology robustness. In this particular case, migration of the metrology process from standard box targets to AIM targets resulted in a 50 percent reduction in overlay model residuals, as shown in Figure 7. A careful inspection of this data also reveals a reduction in the XY asymmetry inherent in the box-in-box residuals.

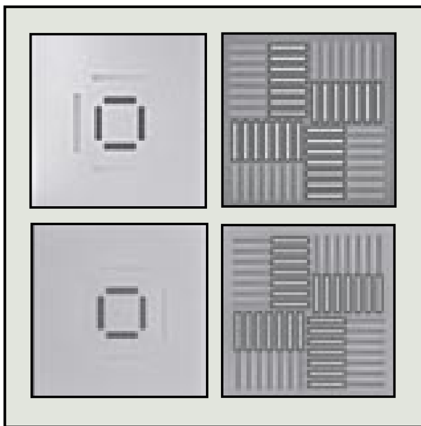

Figure 6. Overlay metrology targets: left box-in-box targets from two different sites on the wafer; right, AIM grating targets from same sites. Box targets suffer from strongly asymmetric contrast variations compared with AIM. Courtesy of ST Microelectronics.

## Conclusions

A DFM approach to overlay metrology dictates an optimization sequence as follows:

1. Optimize model and sample plan for sources of variation.

2. Optimize target for 1 above and for semiconductor manufacturing process.

3. Optimize tool for 1 & 2.

Examples of optimization from steps 1 and 2 have been shown. In the first case it was shown that field-to-field intrafield variability in model terms is a significant contributor to model residuals. Under these circumstances, model and sample optimization is proposed which can potentially improve lot dispositioning and correctibles accuracy. In the second case, target optimization for compatibility with the semiconductor manufacturing process was shown to significantly reduce overlay model residuals and improve residuals XY symmetry.

In the near future, the metrology tools themselves will have to be further optimized not just for reduction in tool uncertainty as quantified in brief evaluations. The optimization metric will be the enabling of a rapid transition to consistent peak performance on process-compatible metrology marks for new and challenging process layers in an expanding repertoire of sample plans.

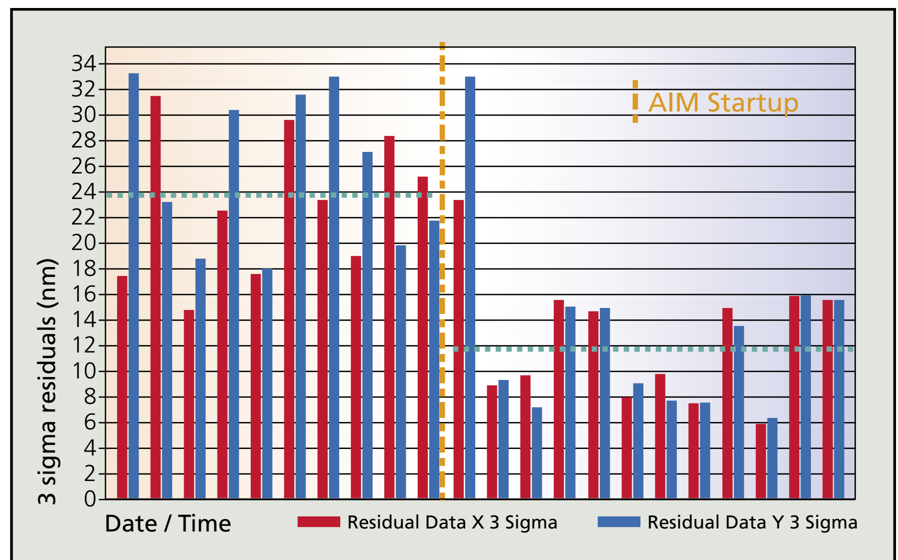


Figure 7. Three sigma overlay model residuals in nm from a 130 nm flash memory process, before and after transition from BiB to AIM based metrology. Data courtesy of STMicroelectronics - R2 Technology Center - FTM - Lithography, Agrate B. Italy.

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**References**

1. A. F. Plambeck, "Overlay metrology as it approaches the gigabit era," Microlithography World, Winter 1996, pp. 17-22.
2. C. Gould, "Advanced Process Control: Basic Functionality Requirements for Lithography," 2001 IEEE/SEMI Advanced Semiconductor Manufacturing Conference, pp. 49-53.
3. International Technology Roadmap for Semiconductors (ITRS) 2004 Update, Section Metrology, p. 6, Table 117a Lithography Wafer Metrology Technology Requirements—Near-term.
4. P. Leray, I. Pollentier, E. Kassel, P. Izikson, M. Adel, B. Schulz, R. Seltmann, J. Krause "In field overlay uncertainty contributors" in Proceedings of SPIE Vol. 5752, Metrology, Inspection, and Process Control for Microlithography XIX, D. J. Herr, Editor, (SPIE, Bellingham, WA, 2005), to be published.
5. M. Adel, M. Ghinovker, B. Golovanevsky, P. Izikson, E. Kassel, D. Yaffe, A. M. Bruckstein, R. Goldenberg, Y. Rubner, and M. Rudzsky, "Optimized Overlay Metrology Marks: Theory and Experiment" IEEE Transactions on Semiconductor Manufacturing, Vol. 17 , No.2, May 2004.
6. M. Adel, J.A. Allgair, D. C. Benoit, M. Ghinovker, E. Kassel, C. Nelson, J. C. Robinson, G. S. Seligman, "Performance Study of New Segmented Overlay Marks for Advanced Wafer Processing," in Proceedings of SPIE vol. 5038 Metrology, Inspection, and Process Control for Microlithography XVII, D. J. Herr, Editor, (SPIE, Bellingham, WA, 2003) pp. 453-463.
7. M. Adel, M. Ghinovker, J. Poplawski, E. Kassel, P. Izikson, I. Pollentier, P. Leray, D. Laidler, "Characterization of overlay mark fidelity," in Proceedings of SPIE Vol. 5038, Metrology, Inspection, and Process Control for Microlithography XVII, D. J. Herr, Editor, (SPIE, Bellingham, WA, 2003), pp. 437-444.

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