(Feed)back to the Future

Enabling Transistor Formation Strategies with Advanced Process Metrics

Kevin Monahan, Umar Whitney – KLA-Tencor Corporation

As super-NA immersion lithography drives CDs smaller, process windows and yield entitlements are also expected to shrink. The prospect of massive transistor-structure-related yield losses at the 45nm node is driving the need for conjoint DFM and APC strategies. The success of these strategies will be critically dependent on feedback of accurate CD, overlay, and film metrology data. This article identifies innovative process metrics and trends, including simulation-based virtual metrology, that promise to be useful enablers for successful next-generation transistor formation strategies.

The primary goal of design for manufacturability (DFM) is to enlarge the process yield window, while the primary goal of multi-variate advanced process control (APC) is to keep the manufacturing process in that yield window (figure 1). This article discusses new technologies that will be needed for increasing yield as innovative transistor structures emerge at the 45nm node and below.

Enabling Transistor Innovation via DFM and APC

DFM requires *feeding forward* design intent, simulator output, layout clips, and design-rule-check (DRC) hot spots to expedite setup of measurement tools. Current DRC and aerial image modeling at best focus and exposure conditions are increasingly unreliable. In the future, process-window-aware approaches will require powerful full-chip simulators that can accurately predict and measure developed patterns in resist, along with *accurate measurement* feedback to calibrate the printability simulator. To control development costs, the conversion of data to information, knowledge, and decisions must be taken as far upstream as possible.

Implementing an APC strategy requires *feeding forward* both process context and measurement data. Looking ahead, we know that process context and measurement data must increase dramatically to support multi-variate control at the lot, wafer, field, die, and intra-die levels. Moreover, yield and performance losses are often caused by process integration issues or combinations of profile, shape, roughness[1],thickness, and pattern placement errors. Combined dispositioning and parametric yield analysis will require data from multiple metrology tools.

The case for linking design, layout, mask, and wafer processes with metrology is compelling. Greater complexity is offset by the advantage of greater access to adjustment. The increasing metrology needs of DFM and APC can be met by innovations in the measurement of pattern shape, profile, overlay, thickness, composition and electrical properties. As an example, examine the transistor drive current equation below:

$$I_d = \frac{1}{2}\left(\frac{W}{L \cdot T}\right) \cdot (\varepsilon \cdot \mu) \cdot (V - V_t)^2 \qquad (1)$$

Drive current at saturation depends on physical dimensions such as gate width W, gate length L, and gate oxide thickness T. It can limit the speed and, therefore, the average selling price of a device. Drive current also varies with electrical properties such as channel electron mobility μ, gate oxide dielectric constant e, and threshold voltage V_t. These are in turn affected by such factors as strain, composition, and transistor architecture. Such performance-driven DFM and APC applications will require new measurement types, creating a need to decrease the cost and increase the yield-relevance of each measurement.

Conjoint APC and DFM Strategies Emerge

DFM and APC are likely to become a conjoint endeavor in the face of increasingly innovative transistor structures, and both will benefit from a wealth of new process metrics. More measurement types, more exotic technologies, and higher sampling will be required to support DFM and APC at the 32nm technology node.

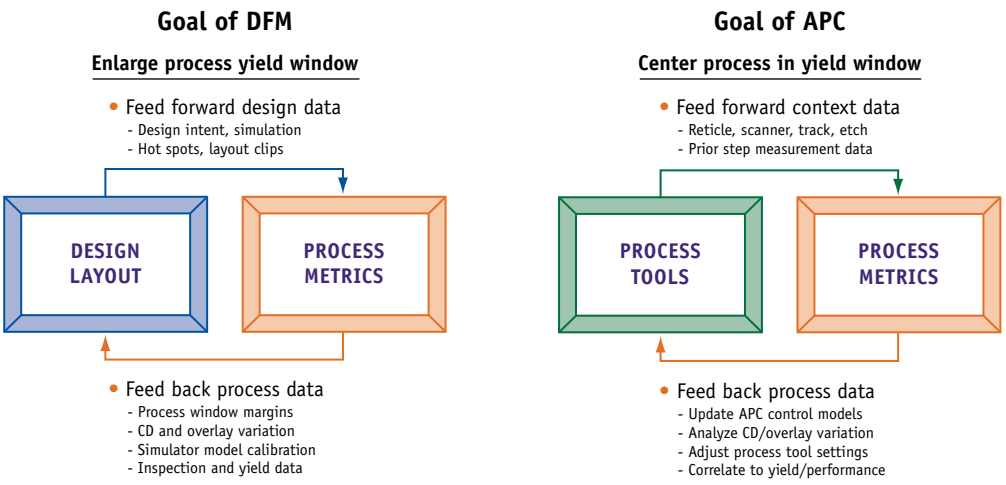

Figure 1: Process metrology is at the center of a conjoint DFM and APC strategy. Both DFM and APC depend on feedback of accurate measurement data and on removing hidden process error.

Some examples are listed below:

- Overlay metrology using tiny, robust grating targets that can be inserted in the device in much the same way that CMP dummy structures are inserted now
- 3D multi-parameter profile scatterometry to measure critical dimensions in advanced planar and non-planar transistor architectures
- Virtual metrology utilizing calibrated litho simulators to assess the printability of complex RET structures, especially those designated for use with immersion lithography
- VUV spectroscopic ellipsometry to measure thickness in complex film stacks on patterned wafers
- Non-contact corona discharge technology to measure leakage and electrical properties of gate dielectrics and the low-k insulators used in advanced interconnect
- Common data analysis platforms with the ability to detect interactions between process errors measured on the same or different tools, especially CD and overlay at 32nm

Changes in the process metrology landscape are accelerating, just as the wavelength reduction roadmap in lithography is decelerating. These changes are driven by the need to fill a widening design-to-process yield gap using DFM and APC strategies. These conjoint strategies, in turn, require new approaches to process measurement:

Advanced Process Metrics for New Transistor Formation Strategies

By accelerating conjoint DFM and APC strategies, the following technologies promise to be useful enablers for transistor innovation at the 45nm node and below:

- Overlay metrology will augment scribe-only applications with in-die metrology, where small amounts of precision may be traded for more representative sampling, large reductions in model residuals, and improved overlay corrections that result in yield improvement.
- CD scatterometry will continue to exploit its advantage in profile metrology and increasingly powerful algorithms that will enable the characterization and control of advanced planar and 3D transistor architectures.
- Simulation will evolve into a calibrated platform for virtual metrology, enabling accurate prediction of downstream measurements due to upstream process variations such as focus or exposure excursions in lithography.
- Ellipsometry is evolving toward in-pattern VUV film thickness metrology and the use of sophisticated algorithms to extract more accurate film thickness measurements in the areas that affect yield most strongly.
- Electrical probe is filling a growing need for non-contact, in-line C-V measurements on new low-k and high-k dielectrics and is finding excursions in electrical characteristics that might otherwise go undetected.
- Data analysis is trending toward common platforms where multivariate techniques can find previously hidden interactions between electrical performance and physical measurements such as CD, overlay, and film thickness.

- ***DFM applications*** such as calibrated OPC/RET verification and design-based metrology (DBM) are developing rapidly. Accuracy is joining precision as a critical parameter for metrology capability, particularly if sub-0.5nm accuracy is required to calibrate OPC/RET models. However, local sample variations such as line-edge-roughness (LER), line-width-roughness (LWR), and film topography may be the ultimate limiters of measurement capability. The need to verify accuracy will continue to drive standards development, but we will also need to understand the "fundamental and practical limits of resolution, accuracy, and precision".
- ***In-die metrology*** with CD SEM is already a required supplement to scribe metrology. Scatterometry (SCD), overlay, film thickness, and non-contact electrical metrology are likely to see more applications in this area. The dimensionality of CD measurement is increasing to the point where shape (SEM) and profile (SCD) are being discussed as targets for APC systems. Along with increased dimensionality, expect to see more use of multiple-measurement strategies and statistical metrology to improve yield-relevance, reduce cost per measurement, and increase overall measurement capability.
- ***Optimal deployment*** strategies are needed for SEM and SCD, as well as a clearer definition of applications for integrated metrology. As SCD takes a greater share of scribe-based APC applications, expect CD SEM to move gradually into the in-die 2D DBM, OPC, and DFM applications. Though SEM offers high-resolution imaging, it is occasionally limited by sample damage, charging effects, and measurement bias. The key advantage of SCD is that it can average over an array of features with high precision and accuracy, but SCD is occasionally limited by parametric model covariance, sensitivity gaps, and interference from underlying layers. Combining SEM, SCD, and other data offers the opportunity to improve overall metrology capability.
- ***Fleet management*** concepts may be extended to multiple metrology tool and data types. Both homogeneous (same tool type) and heterogeneous (e.g., SEM, SCD, AFM) calibration and matching are currently labor intensive. Recipe generation and data analysis are also labor intensive. In the future, data output will be automatically analyzed to select jobs that have the highest robustness to process variation, the most representative sample plans, or the best measurement capability. Tool recipes will reuse common elements and set themselves up without the need for a wafer. SCD could benefit from automated model analysis for parametric covariance, sensitivity gaps, and process robustness. Common analysis of data may also detect CD, overlay, and film interactions that might be yield limiting, especially in the case of dual-exposure, immersion lithography at the 32nm node.

The following sections describe six technologies (figure 2) with significant applications in conjoint APC and DFM strategies, along with key trends that make them applicable for enabling innovative transistor formation at the 32nm node.

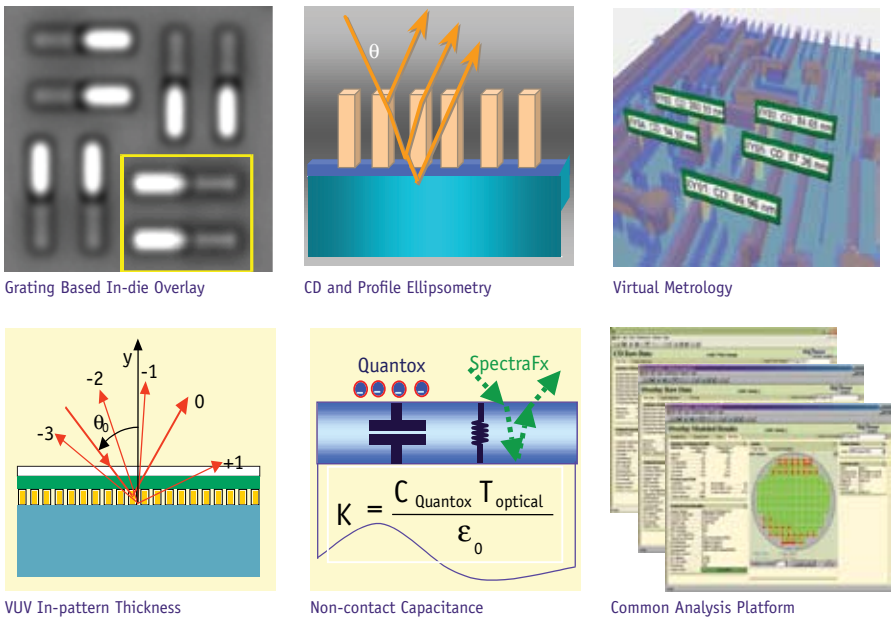

Figure 2: Six technologies with significant applications for transistor innovation at 32nm: in-die overlay, 3D scatterometry, lithography simulation, in-pattern thickness ellipsometry, non-contact electrical metrology, and common analysis capability.

Overlay: From Scribe Line to In-Chip

Traditional box-in-box (BiB) overlay metrology will evolve into more yield-relevant, grating-based overlay metrology (e.g., Archer AIM™). This will take measurement of pattern placement error to new levels of accuracy and enable combined CD and overlay dispositioning. At the 32nm node, BiB overlay metrology will suffer from extreme process sensitivity, particularly with respect to reticle fabrication error, asymmetric deposition and etching, and chemical mechanical planarization (CMP). Grating-based overlay technology (figure 3) can decrease process-induced measurement error by a factor of two. Remaining pattern placement error, including unmodeled intra-chip error, will be addressed

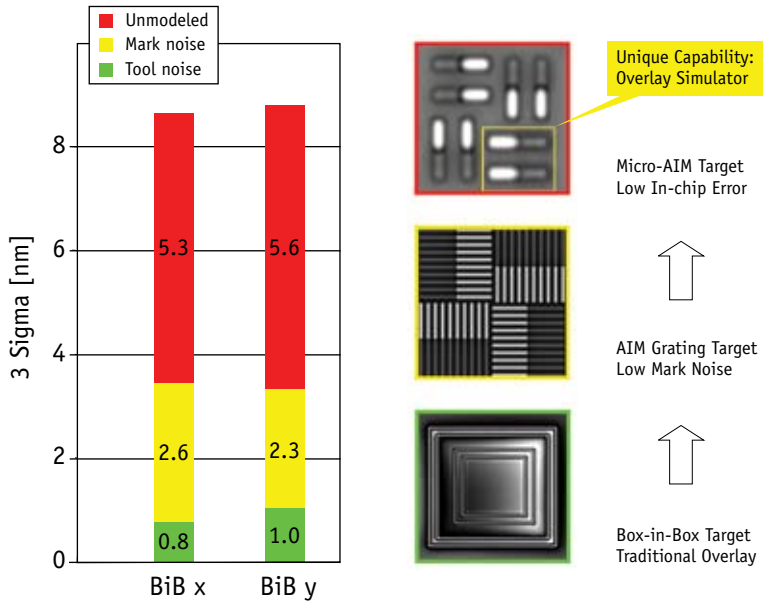

Figure 3: Progression of overlay error reduction strategies from tool noise to mark noise to reduction of model residuals. AIM grating targets reduce overlay mark noise, while in-die micro-AIM targets reduce model residuals, enabling more accurate overlay correction and improved yield.

with tiny in-chip grating targets[2]. These enable more representative sampling and significant reduction of model residuals, arguably the largest remaining source of overlay metrology error. In some cases, such small overlay targets may be combined with line-end-shortening (LES) targets that are used to monitor focus and exposure excursions in lithography cells. The benefits are lower cost per yield-relevant measurement and higher temporal, spatial, and technology correlation for root-cause analysis. At the 32nm node, dual exposure-and-etch strategies may result in direct coupling of CD and overlay error, as in the following equation:

$$CDE = \frac{1}{2} CDE_1 + \frac{1}{2} CDE_2 \pm OLE \qquad (2)$$

The combined CD error (CDE) results from the sum of edge placement errors in the first and second patterning steps, plus an additional contribution from intra-layer misregistration (OLE).

SCD: From CD to Profile Metrology

Scatterometry-based CD metrology (e.g., SpectraCD™) will evolve into more yield-relevant "profile metrology" and may become a reference tool for calibrating CD SEMs down to 13 nm or lower since SCD can accurately reproduce cross-section profiles imaged in a transmission electron microscope. The ability of SCD based on spectroscopic ellipsometry (SE) to accurately measure footing and notching at the base of gate structures has led to two-fold improvements in correlation to electrical L-poly and drive current. For this reason, SCD tools are currently displacing other metrology tools in feed-forward APC applications from lithography to etch. In control applications for shallow-trench isolation (STI), significant cost savings have been realized by metrology convergence. SCD tools are displacing CD SEM, AFM profile, and SE film thickness tools for the control and monitoring of isolation. The benefits are lower cost, shorter cycle-time and greatly reduced temporal, spatial, and technology de-correlation for the more yield-relevant, compound measurements such as aspect ratio. Currently, 3D SCD technology is being applied to measure the profiles and shapes of contact holes and other simple structures. At the 32nm node, the multiple simultaneous measurements provided by 3D SCD may be required for both DFM and control applications.

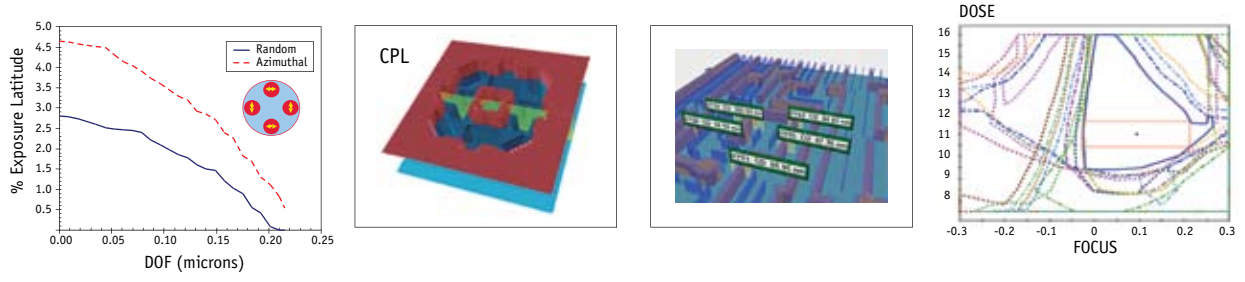

Figure 4: Immersion lithography at the 32nm node will require calibrated simulators that are able to accommodate polarization effects and mask topography. Simulators will be virtual lithography cells that perform virtual metrology on multiple features to find overlapping process windows.

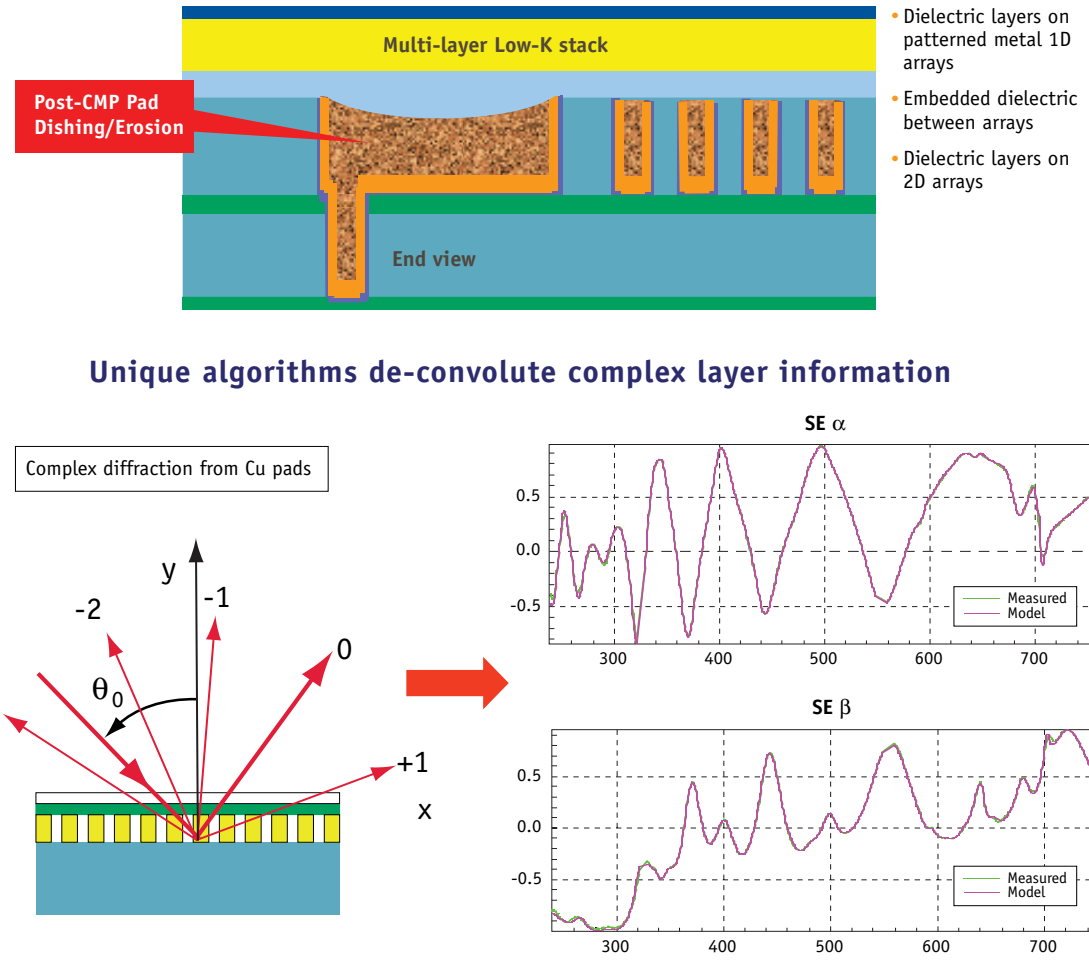

Figure 5: In-pattern film thickness ellipsometry will find increasing application at the 32nm node due to more severe de-correlation of pad measurements with those made in the pattern. In this trend, advanced algorithms would enable de-convolution of complex diffraction patterns from Cu.

Simulation: From Actual to Virtual Metrology

Process modeling and simulation will evolve into yield-predictive "virtual metrology". Even now, the measurement technologies discussed (SEM, SCD, and AIM) rely to some extent on simulation. Simulated SEM images assist with design-based pattern shape metrology. Rigorous coupled wave (RCW) algorithms generate libraries of ellipsometric spectra for comparison with actual SCD data. Overlay simulators[3] predict the optical signatures of innovative overlay targets in order to maximize sensitivity and minimize response to process noise. Finally, robust printability of SEM, SCD, and AIM measurement targets is critical; so calibrated lithography models (e.g., PROLITH™), will be employed to assist in the initial target optimization. These models must use realistic mask data and comprehend the most aggressive resolution enhancement technologies, including immersion polarization and phase shift strategies (figure 4, two left images). Second, they must provide accurate, calibrated results for 193nm immersion lithography and enable rigorous virtual metrology through the focus-exposure window to supplement actual physical measurement (figure 4, two right images). The benefits are lower cost per measurement, in-line validation of physical metrology, and upstream pattern analysis to reduce design, mask, and wafer-level yield loss.

Ellipsometry: From Film Stack to Pattern

Spectroscopic ellipsometry (SE) has been the long-standing best-known-method for measuring the thickness of transparent films used in the semiconductor industry (e.g., SpectraFx™). Expect the wavelength range of these systems to be extended to the VUV, increasing sensitivity to ultra-thin films, high-k gates, high-k memory stacks, and 193nm anti-reflection coatings. Furthermore, in-pattern SE capability will be developed because of the large offsets observed between measurements made on a pad and actual film thicknesses in the die. The extraction of in-pattern thickness will require the use of unique and sophisticated algorithms. Such techniques may be applied to dielectric layers on patterned metal in 1D and 2D arrays (figure 5) and to embedded dielectric between

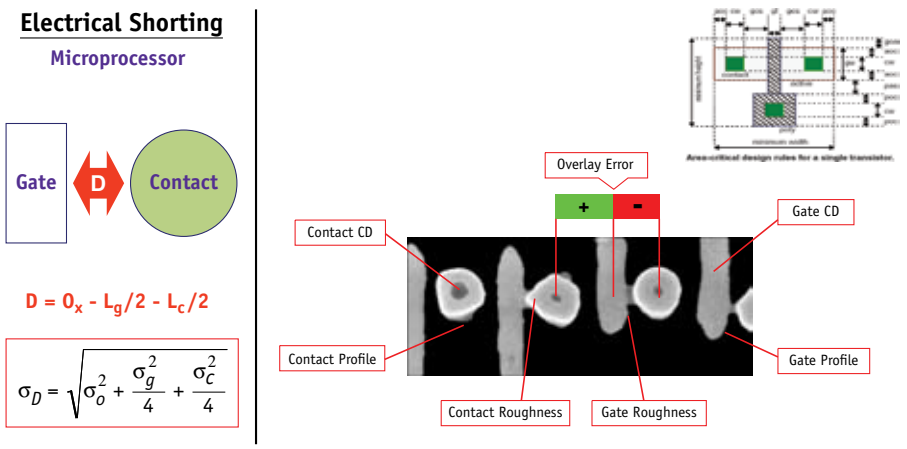

Figure 6: Failure analysis showing gate-to-contact shorting of a device in early development. The design intent for purposes of developing a DFM strategy is shown at the upper right. At least seven overlay, CD, profile, roughness, and topographic errors contributed to these failures.

metal layers. In the front end of the line, prior to STI CMP, in-pattern SE may be used to measure oxide variation as a function of radius across the wafer. At 32nm and below more de-correlation between the on-pad and in-die film thickness measurements will occur, accelerating the trend to in-pattern SE.

Electrical Probe: From Contact to Non-contact

Non-contact electrical probes (e.g., Quantox™) use corona discharge to deposit electrons on the wafer and a Kelvin probe to sense surface voltage and capacitance. This technology replaces contacting C-V measurement with Hg probes and enables in-line monitoring. Major applications are monitoring of low-k dielectric constant, dielectric leakage, and plasma damage in interconnect layers. This technology links synergistically with SE through the equation relating k to capacitance and thickness:

$$k = \frac{C_{Quantox} \cdot T_{SE}}{\varepsilon_0} \qquad (3)$$

Other applications include monitoring of capacitance and leakage of ultra-thin SiON and high-k gate dielectrics. Capacitance and SE thickness measurements can be combined to measure gate dielectric constant. At the 32nm node, on-product monitoring of low-k interconnect and high-k gate dielectrics will be much more critical.

Data Analysis: From One to Multiple Inputs

Advanced parametric analysis (e.g., K-T Analyzer™) is probably one of the most critical functions for accelerating the transition from raw data to actionable knowledge in a factory[4]. Raw overlay data is of little value until fitted to a response surface that furnishes the familiar translation, rotation, magnification, and skew corrections that can be used to adjust a lithography tool. Likewise, a cloud plot of CD variation over time may make little sense until it is broken down by generalized ANOVA into systematic and random components at the cell, lot, wafer, field, and die levels. Another need is the correlation and calibration of physical measurements from multiple sources, such as SEM, SCD, AFM, and TEM. In the case of CD control in lithography, focus-exposure matrices from SEM, SCD, and overlay tools may be fitted to a CD response surface, enabling APC strategies that use feedback of focus and dose corrections. The 32nm node will get much more traction from analysis of correctable interactions between CD, overlay, and films. An example is shown in figure 6, where at least seven overlay, shape, profile, roughness, and topographic errors are interacting to increase the probability of gate-to-contact shorting in a transistor structure.

Conclusions

Virtually all of the technologies discussed above address the problem of hidden process error that could limit yield at the 32nm node. Many systematic variations of concern at 32nm are not observable with in-line metrology tools designed to control current-generation processes. Yield losses due to variation of in-die overlay, pattern profiles, pattern shape, film stoichiometry, in-pattern thickness and electrical properties can only be reduced if they are monitored. Clearly, the extent to which variations and their interactions can be analyzed, simulated, and corrected will determine yield and performance entitlements at 32nm and beyond.

Acknowledgements

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