A Balancing Act

Recent Progress on Strained Silicon Channel Engineering for 65nm CMOS and Beyond

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Much progress has been made by scientists in recent years to overcome the scaling limitation of classical planar CMOS transistors and maintain historical performance trends. New innovations are pushing CMOS transistors to their ultimate limits, beyond any previous predictions, to effectively meet the incessant demand for higher density, performance, and power at lower costs. This article discusses the recent progress made in terms of local and global strained silicon (Si) developments, and their successful insertion into today's state-of-the-art CMOS technologies.

In the 2003 International Technology Roadmap for Semiconductors (ITRS) for CMOS 90nm and 65nm technology nodes, it was projected that neither new materials nor transistor structures were expected for 90nm and 65nm technologies. However, high-k gate dielectrics, dual metal gate electrodes, and elevated source/drain (S/D) structures were expected to extend planar CMOS beyond 65nm. Mobility enhancement – using either biaxial tensile-strained Si thin-film on relaxed SiGe virtual substrate for boosting CMOS performance[1] or selective biaxial compressive-strained SiGe thin-film on Si substrate for boosting performance of p-channel transistor only[2] – was also discussed. It was predicted that these biaxial strained Si or SiGe films would not be qualified for pre-production until mid-2006.

In reality, scaling planar silicon transistors beyond sub-50nm gate lengths (L_g) by increasing the channel and halo doping to suppress short channel effects and controlling off-stage leakage current (I_{off}) has become extremely challenging, if not impossible, without some performance-power tradeoffs. Increasing substrate doping intensifies threshold voltage variation, junction leakage, capacitance, and degradation of carrier mobility. Thus, this approach is not an energy-efficient solution for portable electronic applications. In addition, portable electronics products demand microelectronic chips that are compatible with battery operation over longer and longer time intervals. One facet of the solution is carrier mobility (μ) enhancement. This can boost CMOS device performance (equation 1) without aggressively scaling L_g or gate oxide thickness (T_{ox}) to meet the required performance at lower operating voltage (V_{dd}), while dramatically reducing the active and static power dissipations with low V_{dd} (equation 2).

$$Id_{sat} = W/L * \mu . C_{ox}(V_{dd} - V_t)^2 \quad (1)$$

$$P_{total} = \text{Active Power } (C.V_{dd}{}^2 f) + \text{Standby Power } (V_{dd} . I_{off}) \quad (2)$$

Where Id_{sat} is saturation drain/drive current, W is transistor width, L is transistor channel length, C_{ox} is inversion capacitance, V_t is threshold voltage, P_{total} is total power dissipation, C is total capacitance, and f is operating frequency.

Enhancing carrier mobility can be achieved by several techniques: Uniaxially strained Si using tensile or compressive stressors[3], biaxially strained Si on relaxed SiGe virtual substrates[2], or biaxially strained Si on insulator (SSOI). Innovation while maximizing re-use of existing materials, tools and device platforms has allowed the development of uniaxial stressors that boost both p-type (pMOS) and n-type (nMOS) channel devices in record time. Uniaxial stressors of embedded SiGe in the S/D regions of the bulk pMOS devices[3] were inserted into the mainstream at 90nm in 2004 by Intel, and surely will be used as a p-type mobility booster for high-performance 65nm bulk or SOI circuits by many IDMs[4, 5]. Extensive collaboration among IDMs, equipment and substrate suppliers, consortia, and universities is a critical factor in shortening development cycle times, reducing development costs, and ensuring early entry into mainstream production.

The following sections present recent developments in local and global strained silicon developments, and discuss their effective insertion into cutting-edge CMOS technologies.

Uniaxial Strain

Due to the delay in identifying a pMOS performance enhancement solution, low threading dislocation density (TDD), pile-up defects (PU), and the lack of a cost-effective solution for the biaxial strained Si substrate, novel approaches have been identified and quickly inserted into mainstream products for boosting CMOS performance. These approaches are CMOS-compatible and utilize existing production tools with new processes or modified processes to provide the compressive or tensile stressor, which can boost carrier mobility. Significant stress (tensile or compressive) is imposed on the device in a preferred direction relative to the channel. The strain material distribution is typically localized to impact only one type (p- or n-) of transistor. This is achieved either by stressor incorporation in selected areas, or by locally altering the film characteristics (e.g., strain relaxation by patterned implantation) of an initially blanket stressor film.

Under strain conditions, semiconductor energy bands are shifted relative to each other, and band shapes are changed. When a state is reached with reduced inter-/intra-band scattering or with reduced effective masses, the carrier mobility is enhanced[6]. The impact of strain on carrier mobility can be directly characterized with a piezo-resistance model by measuring mobility characteristics of conventionally built devices under an external mechanical strain. Intensive work has been accumulated in this area, with results characterizing the impact of multiple factors such as device type and channel orientation[3]. Table 1 presents piezo-resistance results as a percentage of carrier mobility enhancement under 100MPa tensile/compressive strain for bulk p/nMOS with <110>/<100> channel orientation. The data is directional for proper uniaxial stressor design. For example, for pMOS with <110> channel orientation, the best mobility enhancement is achieved by adding longitudinal (lateral channel direction) compression, while keeping the stress in the transverse or width direction under tension. However, for nMOS of the same orientation, tension in both channel and width direction is desirable.

Device type	Channel orientation	Longitudinal stress (channel)	Transverse stress (width)	Vertical stress
nMOS	<110>	3.1	1.8	(5.3)
pMOS	<110>	(7.2)	6.6	0.1
nMOS	<100>	10.2	(5.3)	(5.3)
pMOS	<100>	(0.7)	0.1	0.1

Table 1: Percentage mobility enhancement under 100MPa tensile/(compressive) stress.

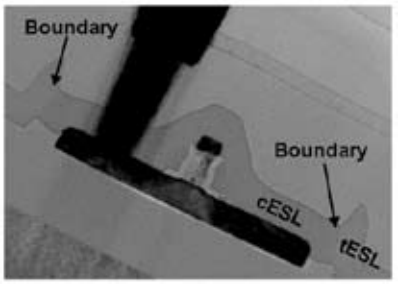

Figure 1: High resolution TEM of an isolated poly pitch, small SA pMOS device in a "compressive-first" dESL stressor.

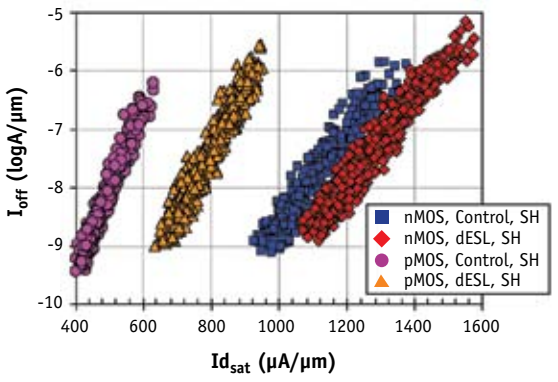

Figure 2: 1.2V pMOS and nMOS self-heated (SH) I_{off} - Id_{sat} curves for dESL integration with -650MPa compressive and +400MPa tensile lateral channel stresses.

Dual compressive and tensile Contact Etch Stop Layer (dESL) or Inter Layer Dielectric (ILD) as stressors have also proven to be viable solutions. Their rapid development times are due to the relative simplicity and reuse of existing manufacturing tools for further enhancing CMOS performance at sub-90nm technologies[3-6], especially when combined in a dual integration scheme[7-9]. Combining the stress sensitivities of <110> channel orientation for pMOS devices with optimized transverse and lateral boundary placement can enhance the dESL performance gains in conjunction with the poly pitch effect[9, 10]. Figure 1 shows a high resolution TEM of the resulting dESL integration on a pMOS device with 70nm lateral boundary spacing. This particular TEM is from an integration in which the compressive film is formed first, and the tensile film second.

Figure 2 illustrates the 1.2V I_{off}-Id_{sat} curves for pMOS and nMOS devices with a dESL integration combining high stress films with +400MPa tensile and -650MPa compressive lateral channel

stresses, respectively. More than 40% Id_{sat} improvement was achieved for pMOS, but less than 10% Id_{sat} gain for nMOS by implementing the dESL stress. As mentioned above, the pMOS device can be enhanced dramatically with a compressive stress in the lateral direction (parallel to current flow). The pMOS devices also prefer tensile stress in the transverse direction (perpendicular to current flow). In dESL integration, this can be achieved by placing the boundary between the compressive and tensile films close to the pFET in the transverse direction. Furthermore, all of these geometry effects need to be accurately modeled to maximize product performance gain.

Other uniaxial stressors can be formed by incorporating an epitaxial stressor layer in pre-recessed device S/D regions. The epitaxial material has a different lattice constant from the substrate. When the atoms of the grown film are well aligned with that of the substrate, and there are no (or negligible) misfit dislocations, the mismatch of the lattice constants of the substrate and refilling materials induces stress to the channel, resulting in mobility enhancement.

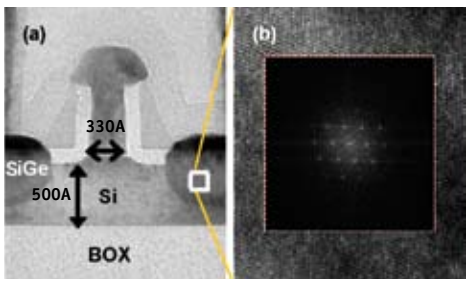

Figure 3: 65nm strained pMOS: a) device structure; b) HR-TEM and Fourier transform diffractogram from S/D SiGe region for crystallinity characterization.

	ΔR_t%	ΔR_{ex}%	ΔR_{ch}%
eSiGe	30.4	32.7	28.2
eSiGe-ESL	39.3	35.8	42.6

Table 2: Improvement on $R_t/R_{ex}/R_{ch}$ from eSiGe and eSiGe-ESL relative to Si reference.

Epitaxial SiGe or silicon carbide (SiC) are the typical stressor materials in this case. SiGe has a larger lattice constant than that of the Si substrate. The S/D embedded SiGe (eSiGe) therefore induces the desirable lateral channel compression, while the S/D embedded SiC induces channel tension, which enhance hole or electron mobility and drive current of the transistor, respectively. Many reports on pMOS S/D eSiGe stressors have been disclosed in recent years for bulk and SOI technologies. Ghani et. al. reported that eSiGe for 90nm node bulk circuits were in production in late-2003[3]. To couple eSiGe performance enhancement and SOI substrate benefits, Zhang et. al. reported an eSiGe stressor on a 65nm SOI platform (figure 3), with at least 20% gain in drive current and Id_{sat}, as shown in figure 4[11]. Higher Id_{sat} gain, up to 45%, can be accomplished by reducing the SiGe offset relative to the gate or by the increasing the Ge concentration.

Figure 4 shows that coupling of the eSiGe stressor with a compressive dESL stressor results in nearly linear enhancement combination, and more than 50% pMOS Id_{sat} enhancement is demonstrated. The drawback of the uniaxial stressor is its strong dependence on geometry factors such as gate spacing, device width and density (figure 5). The study shows that incorporating eSiGe is important to maintain appreciable Id_{sat} improvement at narrow device width, while the performance gain by dESL decays as device width dimension decreases.

Additional important benefits of the eSiGe stressor include its ability to retain hole mobility gains at high vertical fields, and to reduce device channel resistance (R_{ch}) and extension resistance (R_{ex}). This investigation shows that eSiGe not only

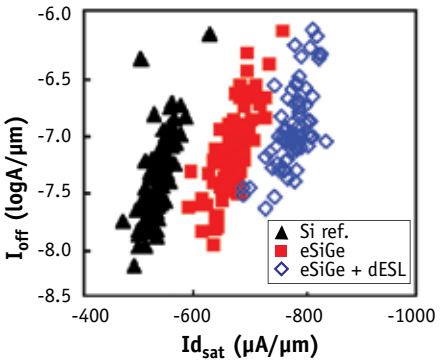

Figure 4: Off current as a function of drive current for strained and unstrained pMOS devices.

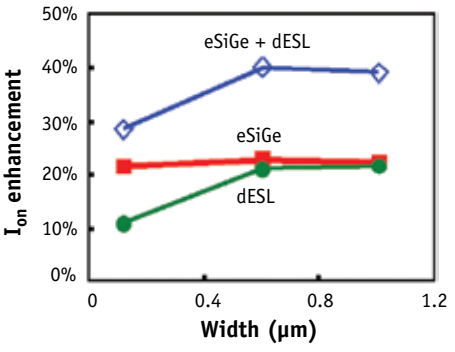

Figure 5: I_{on} enhancement as a function of device width for different strained devices.

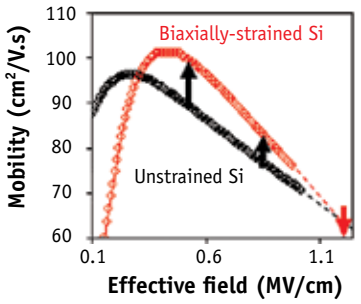

Figure 6: Long-channel hole mobility showing the strong sensitivity of the biaxially strained Si enhancement as a function of effective vertical field.

enhances the mobility but also reduces both R_{ch} and R_{ex} while the compressive ILD stressor only reduces R_{ch} (table 2). Processes and mechanisms that are similar to eSiGe, but that use tensile embedded SiC in the S/D region to boost n-type transistor performance, have received much recent attention due to the similarity to the existing eSiGe module, and have demonstrated potential for large performance gains up to 30% due to electron mobility enhancement[11].

Biaxial Strain

When a thin Si layer is grown pseudomorphically on a relaxed SiGe alloy buffer having larger lattice spacing than that of Si, the Si layer conforms to the SiGe template by expanding laterally and contracting vertically. This creates a biaxial stress, which enhances the transport properties of the Si layer due to altered band structure and electronic properties compared to unstrained Si. Stress reduces inter-valley and inter-band phonon scattering and effective hole mass due to band warping and preferential thermal population of electron states with

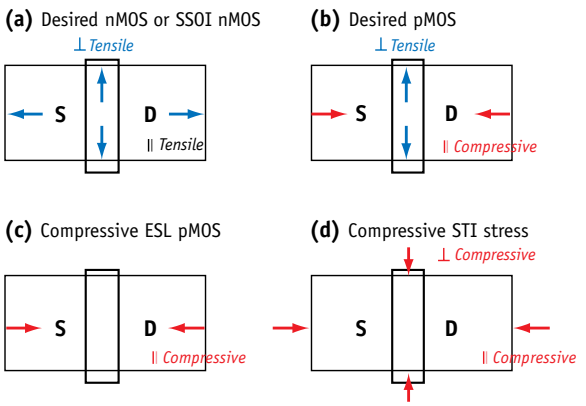

Figure 7: Schematic showing various stress configuration and their associated stressors.

light transport effective mass. Improvements to both electron and hole mobilities by applying biaxial tensile-strained Si as a transistor channel have been demonstrated[13]. However, the fundamentally weak pMOS enhancement will pose scaling difficulties for global biaxial stressors in high performance CMOS. Although biaxial tension can produce modest hole mobility enhancement at low vertical effective fields, channel carrier sub-band splitting due to biaxial stress and its associated effective mass change[14] leads to an undesired enhancement sensitivity to the vertical effective field (figure 6). The hole mobility

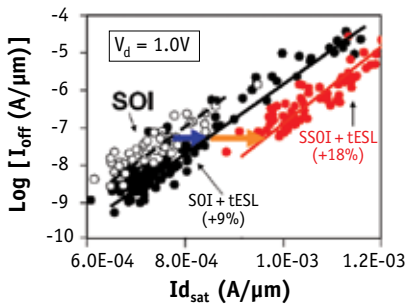

Figure 8: Id_{sat} - I_{off} plot showing the nFET enhancement due to tESL & SSOI.

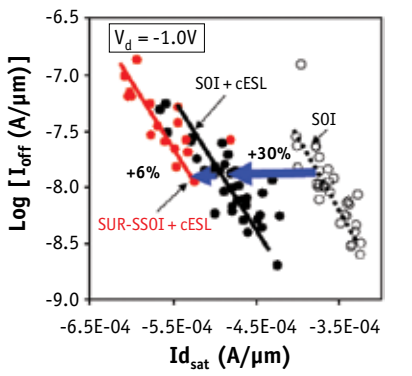

Figure 9: Short-channel pFET Id_{sat} - I_{off} plot showing the enhancement due to SUR and cESL (W = 1µm).

enhancement under high effective gate fields is diminished and becomes negative when the fields are high. Piezo-resistance coefficients show that strong pMOS enhancement results when the undesired tension along the channel is reversed (table 1). Moreover, the transverse tension along W should be preserved for pMOS performance[15]. A novel in-plane stress engineering approach achieves the desired CMOS stress configuration as shown in figure 7, which would be more difficult to achieve by purely using uniaxial or biaxial stressors[16]. The interactions and optimization between biaxial-uniaxial stresses-relaxation

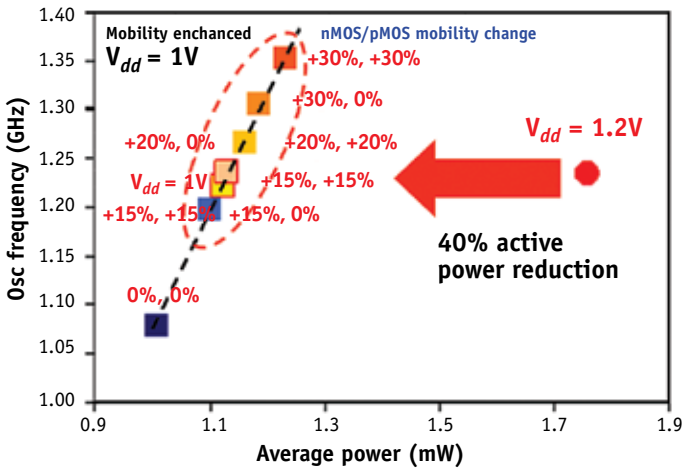

Figure 10: Circuit simulation of phase-locked loop (PLL) core block ring-oscillator with 356 SOI MOSFETs and ~2000 resistors and capacitors similar to a core block in PLL circuits.

and channel directions to obtain optimum performance gain for 65nm CMOS device has been proven (figures 8 and 9)[17]. Circuit simulation indicates that the logic circuits could achieve 1.2V circuit speed with 1V supply and 15% mobility for both n- and p-type transistors, and 40% dynamic power reduction at the same frequency (figure 10). Important progress has been made by SOI vendors in improving quality, availability and cost of SSOI substrates. Recent progress in TDD reduction and PU elimination is also promising, since these defects are potential yield killers, and also adversely impact device leakage and power dissipation.

Conclusion

Uniaxial stressors have been employed for boosting mostly pMOS performance. It will be more difficult to improve nMOS performance using the tensile stressor until cost-effective and manufacturable selective embedded SiC process and dual embedded S/D stressors integration are available. This implies changing the n:p ratio with technology scaling, which requires extensive library and circuit layout changes. Enhancing both nMOS and pMOS performance to retain the same n:p ratio is desirable. Interactions between biaxial lattice strain, uniaxial relaxation, process-induced stressor and channel orientation have been optimized to achieve the desired stress configurations for enhancing both short-channel SSOI nMOS and pMOS devices. Significant progress has already been made in meeting the performance, power and cost requirements for SSOI technology by joint collaboration between IDMs and substrate suppliers during the SSOI development and assessment phase.

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