Process Watch: Hitback Analysis Improves Defect Visibility

By Chet Lenox, David W. Price and Douglas G. Sutherland

Author's Note: The Process Watch series explores key concepts about process control—defect inspection and metrology—for the semiconductor industry. Following the previous installments, which examined the 10 fundamental truths of process control, this new series of articles highlights additional trends in process control, including successful implementation strategies and the benefits for IC manufacturing. For this article, we are pleased to include insights from our guest author and colleague at KLA-Tencor, Chet Lenox.

In order to maximize the profitability of an IC manufacturer's new process node or product introduction, an early and fast yield ramp is required. Key to achieving this rapid yield ramp is the ability to provide quality and actionable data to the engineers making decisions on process quality and needed improvements.

The data used to make these decisions comes in two basic forms:

- Inline inspection and metrology results
- End-of-line (EOL) parametric testing, product yield results and failure-analysis

Inline inspection and metrology serve as the primary source of data for process engineers, enabling quick identification of excursions and implementation of corrective actions. End-of-line results serve as a metric of any process flow's ability to produce quality product, generating transistor parametrics, yield sub-binning and physical failure analysis (PFA) data that provide insight into process quality and root-cause mechanisms.

In general, a fab is better off financially by finding and fixing problems inline versus end-of-line[1] due to the long delay between wafer processing and collection of EOL data. However, EOL results are a critical component in understanding how specific inline defects correlate to product performance and yield, particularly during early process development cycles. Therefore, the ideal yield improvement methodology relies on inline inspection and metrology for excursion monitoring and process change qualification, while EOL results are used only for the validation of yield improvement changes.

In order for this scenario to be achieved, inline data must be high quality with appropriate sampling, and a clear correlation must be established between inline results and EOL yield. One key tool that is often utilized to achieve this connection is **hitback analysis**. Hitback analysis is the mapping of EOL electrical failure and PFA locations to inline defect locations identified by inspection tools.

Hitback analysis comes in two basic forms. In the traditional method, EOL yield failures guide PFA, often in the form of a cross-section transmission electron microscope (TEM) confirmation of a physical defect. This physical location is then overlaid against inline defect locations for correlation to inline learning. This analysis often offers clear causality for yield failures, but is slow (dozens/week) and can be blind to defect modes that are difficult to locate or image in TEM.

The second method, which is growing in popularity, is to overlay the EOL electrical failure location directly to inline defect data (figure 1). This is largely enabled by modern logic design methods and analysis tools that allow electrical failures to be localized into "chain" locations where the failure is likely to occur. Furthermore, new technologies allow inline inspection to be guided to potential chain location failures based purely on design layout.

For example, KLA-Tencor's broadband plasma optical patterned wafer inspection systems incorporate patented technologies (NanoPoint™, pin•point™) that leverage design data to define very tiny inspection areas focused solely on critical patterns.[2,3,4] Using these design-based technologies to inspect patterns related to potential chain failures produces inspection results consisting of defects that are strongly correlated to end-of-line yield. This more direct technique allows for faster turn-around on analysis, enables higher sampling (hundreds of defects/wafer) and can provide successful causality on defect modes that are difficult to find physically at EOL.

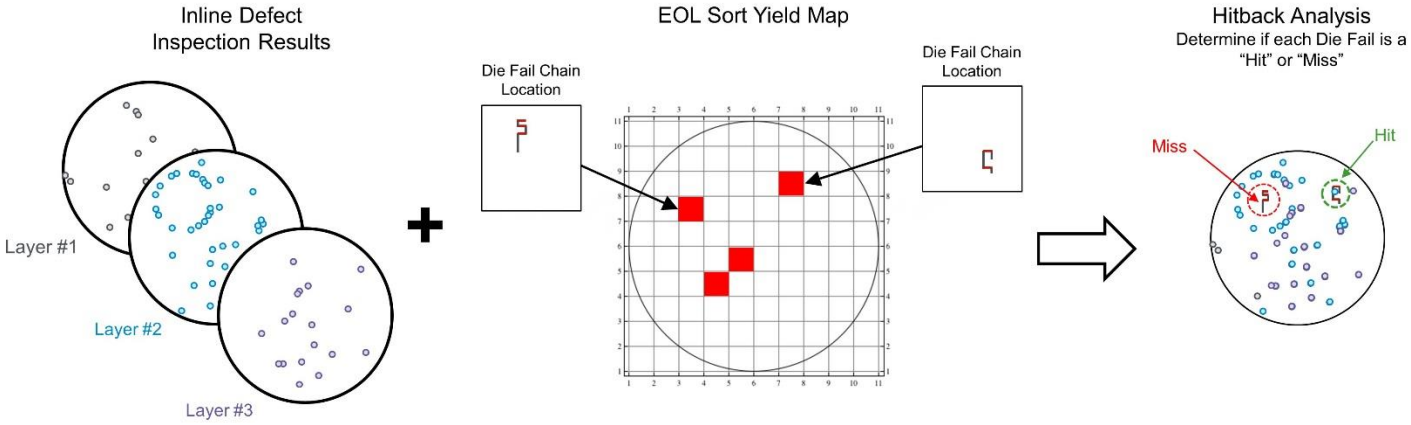

Figure 1. Hitback analysis technique where likely die fail chain locations from EOL are overlaid with inline inspection results.

To achieve successful direct hitback analysis from electrical fail chains to inline defect locations, a number of methodologies are helpful:

- Wafers that will be used for hitback analysis should be inspected at all key process steps. This avoids “holes” in potential causality to the EOL failure
- Geometry-based overlay algorithms should be used that combine the point-based inline defect location with area-based reporting of EOL chains
- The overlay distance allowed to label a chain-to-defect distance a “hit” must be large enough to allow for inspection tool defect location accuracy (DLA) but small enough that the statistical probability of false-positives is low; see Figure 2
- All defects found by the inspector should be used for analysis, not just defects that are classified by subsequent review steps
- Electrical fail chain locations should utilize layer information as well as x/y mapping

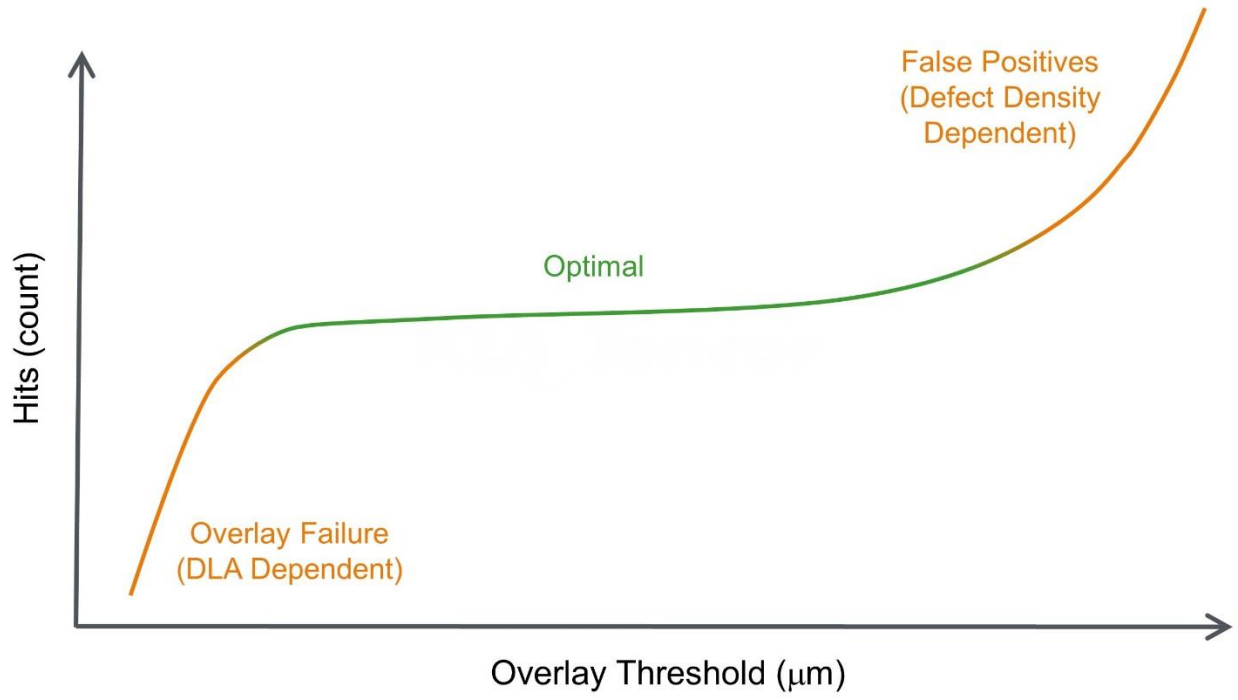

Figure 2. The threshold used to overlay EOL electrical chains to inline defects must be optimized to avoid failures or false positives.

When performed properly, the hitback capture rate metric (in percentage) will quantify the number of fails which “hitback” to inline defects. This metric can be used broadly as an indicator of inline inspection capability, with higher numbers indicating that inline inspection can be more confidently

used in yield improvement efforts. Therefore, hitback analysis should be performed as early as possible in the development cycle and new product introduction timescale. This allows time for inline defect inspection capture rate improvement through these traditional methods:

- Inspection tool and recipe improvement, including the use of guided inspection based on product layout
- Lot-, wafer- and die-level sampling adjustments
- Process step inspection location optimization

When performed regularly, hitback analysis greatly assists in improving inline inspection confidence and improves yield learning speed. Hitback capture rates increasing to more than 70 percent are not uncommon for effective inline monitoring schemes. It is worth mentioning that the slower EOL PFA Pareto generation and hitback analysis is still required even when direct EOL-to-inline is performed in order to validate the chain fails and hitback capture rate.

Yield ramp rate is often the primary factor in the profitability of a fab's new process and new product introduction. This ramp rate is strongly influenced by the effectiveness of inline wafer inspection, allowing faster information turns and quicker decision making by process engineers. Hitback analysis is a key method for gauging the effectiveness of inline inspection and for driving inspection improvements, particularly when correlating EOL electrical chain failures to inline defect results.

References:

1) Process Watch: The Most Expensive Defect, *Solid State Technology*, December 2014
2) "Introduction to NanoPoint," http://www.kla-tencor.com/index.php?option=com_joomdoc&task=document.download&path=NanoPoint_Overview.pdf
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Dr. Chet Lenox, Dr. David W. Price and Dr. Douglas Sutherland are Yield Consultant, Senior Director, and Principal Scientist, respectively, at KLA-Tencor Corp. Dr. Lenox, Dr. Price and Dr. Sutherland have worked directly with many semiconductor IC manufacturers to help them optimize their overall inspection strategy to achieve the lowest total cost. This series of articles attempts to summarize some of the universal lessons they have observed through these engagements.