

The Power of Innovation

Judging from the technology news hitting the wires as I write this in mid-June, low power consumption was the overarching theme at the 2006 *Symposium on VLSI Circuits*. At the conference, leading companies such as Texas Instruments, IBM, Intel, IMEC, Freescale Semiconductor and others presented compelling, and often competing, visions on the future of the transistor. One headline in particular – Paths Diverge Toward Next-Gen Transistors – caught my attention.

Everything, of course, relates back to the stalling of CMOS performance largely because of the practical limits on power consumption in computers and mobile applications. As an IC Insights analyst puts it, “The power transistor market is set to drive the market to record levels in 2007.”

Given both the unprecedented interest in the future of the transistor and its role as the heart of consumer-driven applications we, at *Yield Management Solutions*, feel strongly about creating an issue with a special focus on transistor innovation. Our cover story, IMEC’s “Raising the Bar” leads the way towards creating metal gate electrodes with a fully silicided approach as a practical solution to continue transistor performance scaling.

New innovations are pushing CMOS transistors to their ultimate limits so they can effectively meet the incessant demand for higher density, performance, and power at lower costs. In “A Balancing Act,” Freescale Semiconductor discusses the recent progress made in terms of local and global strained silicon developments, notably enhancing carrier mobility, for boosting CMOS device performance without disrupting the delicate balance of power.

Freescale Semiconductor strongly believes that “extensive collaboration among IDMs, equipment and substrate suppliers, consortia, and universities is a critical factor in shortening cycle times, reducing development costs, and ensuring early entry into mainstream production.” This is an easy segue into important facets of semiconductor innovation: How do we know if it is economically feasible? Will the current process control technologies provide the required level of insight into the issues? Will new manufacturing challenges require innovative yield management technologies and strategies?

To date, laser-based darkfield inspection tools filled a key role in semiconductor inspection by providing high-throughput defect monitoring capability. As the industry moves beyond 65nm design rules and grapples with new challenges and continued cost pressures, conventional darkfield inspection technology struggles to meet manufacturers’ demands for cost effective inspection that provides the required sensitivity at production throughputs. “The Winning Streak” examines an innovative inspection technology that combines laser-based inspection with new darkfield imaging technology. Bolstered by

years of technology innovation experience, the sky is the limit insofar as the range of applications that can be cost effectively addressed with this new inspector.

As clichéd as it sounds, knowledge *is* power. And we find knowledge in unexpected places. Previously, surface scattering was viewed mainly as a noise source for optical wafer inspection. More recently, wafer manufacturers and their customers used surface scattering measurements as a simple, single-value representation of surface quality, to accept or reject wafers. “Surface Watch” unveils a new product that leverages the system architecture of KLA-Tencor’s unpatterned wafer inspector to deliver surface-scattering data at unprecedented sensitivity. The measurement sensitivity of this system can be applied to detect changes in surface roughness for various surface types. This provides a wealth of information that is valuable for process development and may even be used for process monitoring.

Looking ahead, the prospect of massive transistor structure-related yield loss at the 45nm and 32nm node is driving the need for conjoint DFM and APC strategies. “(Feed)back to the Future” presents a compelling argument for linking design, layout, mask, and wafer processes with metrology. The article discusses in great detail how the increasing metrology needs of DFM and APC can be met by innovations in the measurement of pattern shape, profile, overlay, thickness, composition, and electrical properties.

Many articles in this issue present practical and innovative yield management approaches that have been successfully applied in production.

Clearly, if innovation is the key to our industry’s future, we must continue to work together (even if we don’t always agree) to enable radical new transistor technologies and structures that will ultimately revolutionize our world.

Vive L’innovation!



A handwritten signature in black ink, which appears to read "Uma Subramaniam".

Uma Subramaniam
Editor-in-Chief