Methodology for Trench Capacitor Etch Optimization using Voltage Contrast Inspection and Special Processing

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Abstract – **Embedded DRAM will play a much larger part in IBM server microprocessors for new SOI technologies. Etch of a deep trench (DT) into the substrate, which is used to form the capacitor, is a complicated multi-step process. One of the key elements is etch of the buried oxide layer. Voltage contrast (VC) inspection is used to detect defective DTs and can differentiate between opens in the buried oxide and those in the oxide hard mask. So these defects have a VC signal, special processing is needed to seal off the SOI layer. The process of finding the right beam conditions to detect the opens in the buried oxide, which are very subtle, is described. Failure analysis of these defects is also presented.**

I. INTRODUCTION

Embedded dynamic random access memory (eDRAM) provides unique advantages over static random access memory (SRAM) for use in certain memory caches for IBM server microprocessors. This is because each bit takes approximately 1/3 the area and therefore a much larger amount can be embedded in a constrained space. Even with the periphery circuitry required to refresh the eDRAM, the space savings is still substantial. Therefore IBM has invested substantial effort to develop robust EDRAM modules for recent SOI technologies [1,2].

The IBM eDRAM scheme uses capacitors that are formed into the wafer substrate; hence they are called deep trench capacitors (DT). A trench is etched through the buried oxide (BOX) and very deep into the substrate. One of the major challenges for this module is optimization of the multi-step etch process which breaks through the BOX. The timing and chemistry of each component of this etch sequence must be tuned to uniformly etch through the particular layer it targets.

Figure 1 shows a diagram of several DTs after the BOX open etch. One is good and the other is bad in that it failed to break through the BOX. The ability to detect these bad DTs from a large population of good DTs at this point in the process would enable a fast feedback loop for process tuning. The natural technique to use for this purpose is VC inspection. This is because VC inspection has proven very successful for detecting a wide variety of other yield loss mechanisms in-line at level [3-8].

The initial thought was to inspect right after the DT BOX open etch step. This however was not successful because grounding is provided by both the substrate and the SOI layer. Since even most bad DTs have hit the SOI layer, good and bad DTs cannot be differentiated.

One of the next process steps in the process sequence is to line the DTs with a dielectric. This seals off the SOI layer as well as the substrate. This is followed by the DT main etch step, which first breaks through the thin dielectric layer at the bottom of the DT before etching the DT trench into the substate. The liner sealing off the SOI layer remains intact. Our solution was to run just this first component of the main etch sequence, called break-through etch, and then inspect the wafers. Figure 2 shows a diagram of good and bad contacts at this point. Stopping the processing at this point is non-standard and therefore these wafers are considered sacrificial. At some point it might be possible to qualify a process where the main etch is split in two with an inspection in between.

Our efforts to find the optimal inspection conditions for detection of DT opens after the break-through step are described in Section II. The failure analysis (FA) used for verification of these defects is described in Section III. This inspection has been used for optimization of the DT mask open etch process. These studies are still on-going.

II. RECIPE DEVELOPMENT

A. Apparatus

A KLA-Tencor eS35 inspection SEM was used for this work. These studies were conducted at IBM's E. Fishkill semiconductor fab using 32SOI technology.

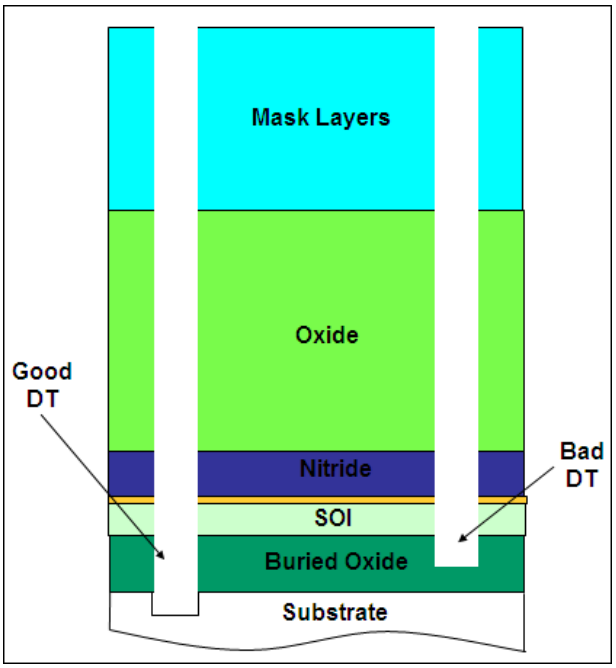

Figure 1: Good and bad DTs after DT BOX open etch

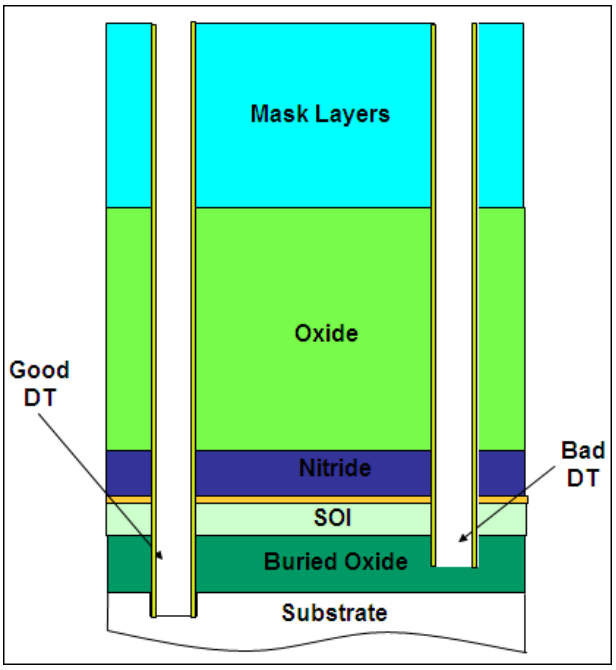

Figure 2: Good and bad DTs after liner deposition and break-through etch

B. Inspection Settings Optimization

Initially, conditions were selected to isolate defects like the one in Fig. 3. This defect has a very strong VC signal. The area containing this defect was polished to below the BOX. Figure 4 shows that one DT is indeed missing. Since it was visible at the wafer surface, this indicated that the bad DT was formed but did not make it to below the BOX. Our early belief was that this defect corresponded to a DT open in the BOX (BOX Open) like the one on the right in Fig. 2. Subsequent FA, showed that this strong VC defect is a DT that stopped in the oxide (Oxide Open), well above the SOI. Based on this, additional beam optimization work was undertaken to bring out more subtle defects.

The eS35 has a "beam optimization" feature where the signal to noise can be compared for a particular defect for a variety of different beam conditions. Also the grey level of a particular defect can be compared to neighbors using a histogram function. Both of these features were used to select optimal e-beam conditions. First, though, candidate conditions needed to be selected.

Jau *et. al.* and Lei *et. al.* discuss inspection of etched vias prior to fill [9,10]. These references show that vias that are just barely open (i.e. just a small amount of oxide remaining that they did not get through) can be differentiated from hard opens. This situation is very similar to the DT opens of interest in this paper. Hard open vias will appear very bright because most electrons cannot penetrate the remaining dielectric and a lot of negative charge builds up at the wafer surface. For slightly under-etched vias, many electrons will penetrate through the remaining dielectric, but some will not. Therefore a slight negative charge builds up and the contact appears grey. For a fully etched vias, all or at least most of the electrons reach the conductor underneath the via. Very little charge builds up and these vias appear dark. Jau *et. al.* reports using a low landing energy (LE). This maximizes the number of electrons that did not penetrate the remaining dielectric for slightly under-etched vias, allowing them to be differentiated from full etched vias. Based on this information, we primarily focused on lower LEs to differentiate between good DTs, BOX Opens and Oxide Opens.

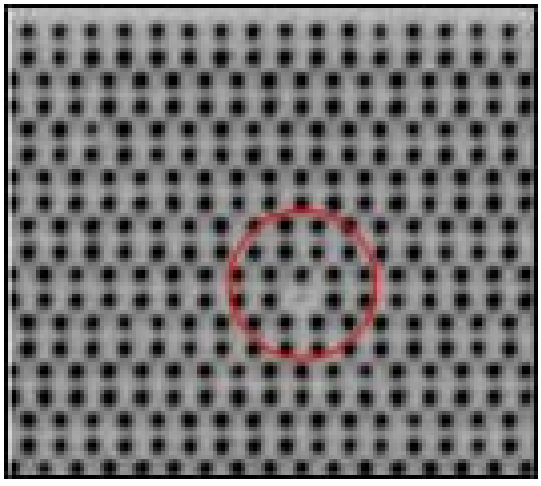

Figure 3: e-beam image of a bad DT.

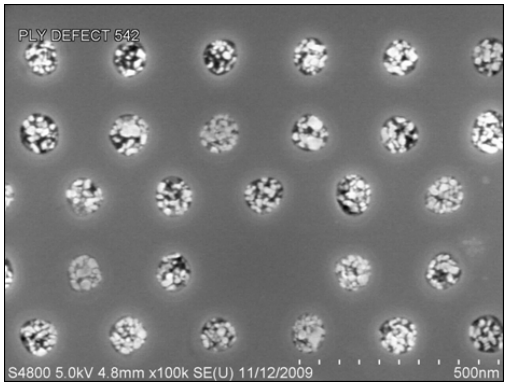

Figure 4: Top down SEM image of location of defective DT after polishing to below the BOX.

To maximize the sensitivity to slight grayscale differences, a relatively small pixel size was used compared to the DT critical dimension (CD). Because a slight difference in grey scale between BOX opens and good DTs was expected, multiple pixels must fall within the center of the DT. Figure 5, which shows a simulated image of 40nm round defect, illustrates this idea. In this simulation, the grey scale value within the defect is 10 greater than the value outside the defect. Figure 5 shows the pixel maps for 10nm, 20nm and 30nm pixel size. White represents 0-3, light grey represents 4-6 and dark grey represents 7-10. If only the dark grey is above the threshold, then the detected defect size shrinks to zero with a 30nm pixel. The 10nm pixel size is the best choice.

Typically for defects with a strong VC signal (i.e. large grey scale difference from the reference image), a pixel size similar to or even larger than the CD is typical. The grey scale range in Fig. 5 might be 3x larger. Therefore the light grey regions could also be detected. In this case, the 30nm pixel size is the best choice of the three options. Beam current (BC) must follow the selection of pixel size. Larger BCs create larger spot sizes. A smaller spot size and therefore BC was selected to keep the spot size comparable to the pixel size. The image resolution is a good empirical indicator of when this occurs. Too low of a BC results in the loss of VC signal. This is because a good flow of electrons is necessary to charge up floating electrical nodes. Therefore, the BC should be small enough to get sufficient resolution, but no smaller.

Figure 5: Simulated image of a 40nm round VC defect with three different. pixel sizes. Left – 10nm, Middle – 20nm, Right – 30nm.
If only the dark grey is above the threshold, then the detected defect size shrinks to zero with a 30nm pixel.

Beam optimization focused on LEs in the range of 100 to 500V and Wehnelt (W) voltages in the range of 0 to 500V. Based on the defect image, 25nA was determined to be the best BC. For the optimization work, a higher number of image averages was used to reduce the noise. The actual production inspection would use a much lower number. The candidate conditions used included:

350LE 500W 25BC
100LE 500W 25BC
500LE 100W 25BC

A region of EDRAM imaged with each of these conditions is shown in Figs. 6a, 6b and 6c. Figure 7 shows the 350LE_500W_25BC condition image marked with circles showing the suspected location of the BOX opens. The grey scale was analyzed for the circled DTs versus other DTs using a histogram function available on the eS35. Figure 8 shows two example 350LE_500W_25BC histograms. The un-circled DT's average grey scale value ranged from 87 to 92, whereas the circled DT's average grey scale value ranged from 114 to 120. This indicates that a signal can be seen above the noise level. The beam optimization function of the eS35 was used to select the best beam condition to detect these defects. The 350LE_500W_25BC condition was selected.

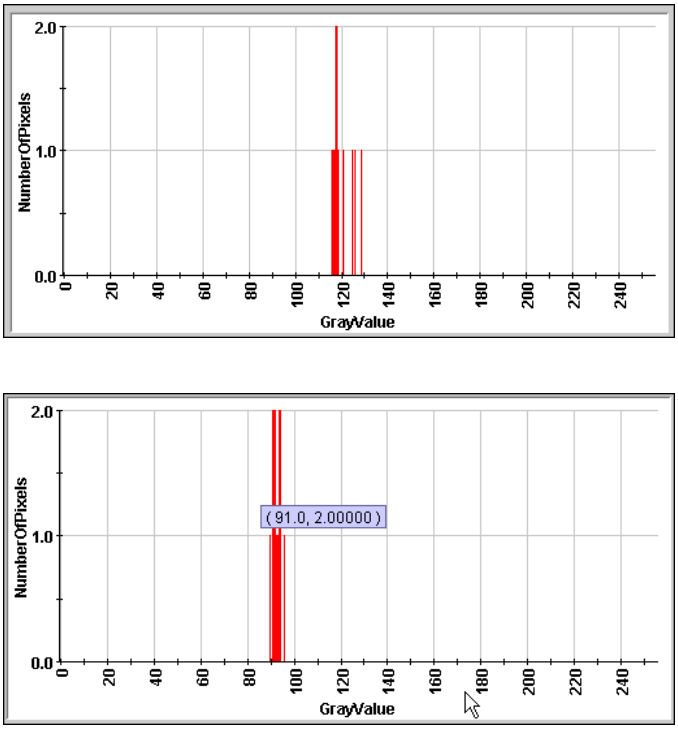

Figure 8: Example histograms for a circled DT (top) and an uncircled DT (bottom).

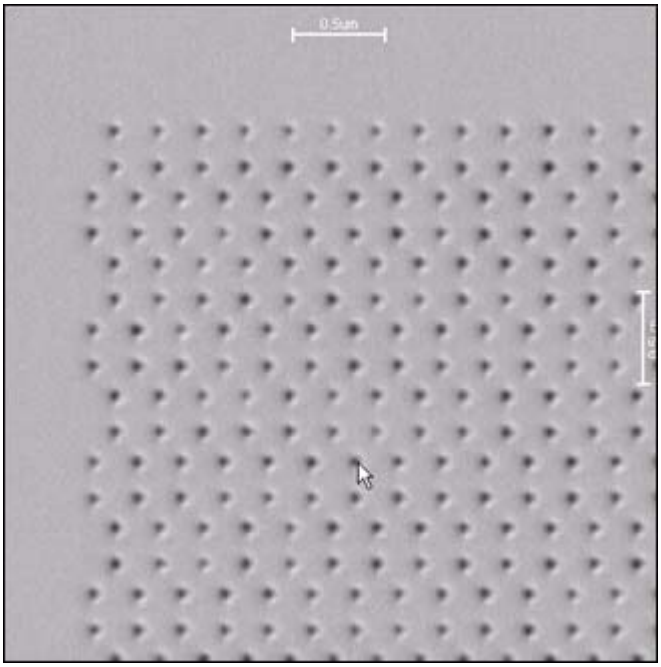

Figure 6a: 350LE _ 500W_25BC

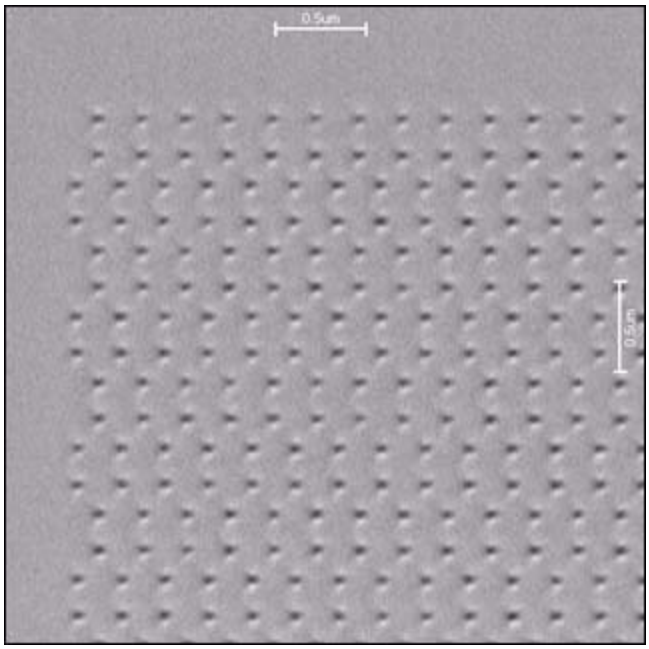

Figure 6c: 100LE _ 500W_25BC

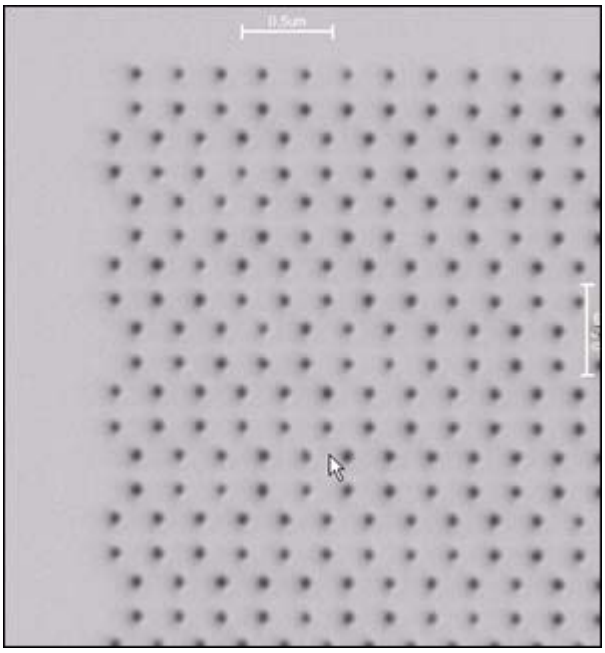

Figure 6b: 500LE _ 100W_25BC

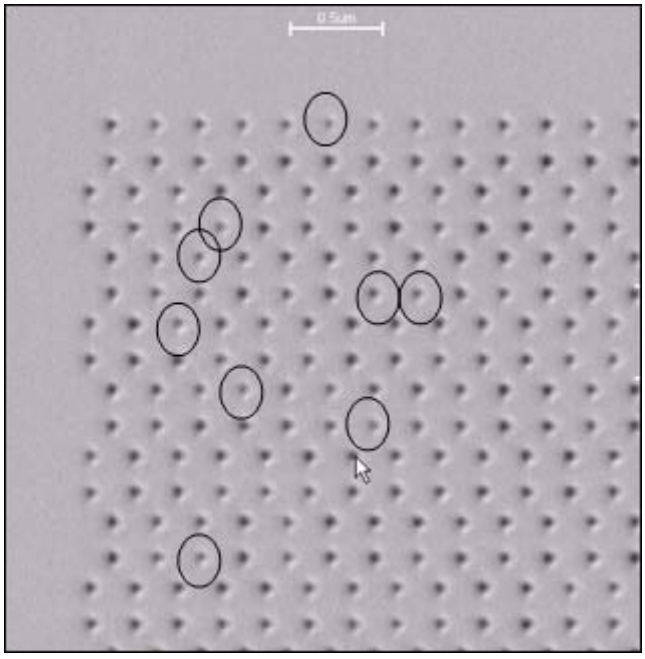

Figure 7: 350LE _ 500W_25BC with suspected BOX Opens marked.

III. FAILURE ANALYSIS

To verify these e-beam defects are indeed bad DTs, several failure analysis approaches were taken. First, as mentioned in Section B, a top down polishing technique was used, where the wafer was polished to a level just below the BOX and then imaged top down. The problem with this technique is that it does not differentiate between Oxide Opens and BOX Opens. Next, FIB cross sections were used, where a FIB cuts the cross section and then a SEM beam takes images. Figure 9 shows an example. The problem with this technique is that the FIB leaves artifacts, which makes interpretation of the DT depth difficult. Material can be deposited and/or removed.

Ultimately for this defect type, hand polished cross-sections were utilized. The challenge with this method is hitting the failing DT. The FIB is still necessary to create cross-hairs marking the fail location, but a layer of chrome can be deposited beforehand to protect the DT's from the FIB beam. The following procedure was used:

1. Sputter coat with two minutes of chrome. This protects the defect from the FIB beam while generating marks necessary to locate the fail.
2. Drive to the general fail location with the FIB using the x,y coordinates from the eS35 data. Once the fail is identified, the FIB is used to mark the fail as shown in Fig 10. Minimal scans are used to limit damage from the beam. Additional laser marks are added later to aid in navigation. These are the larger square marks.
3. Deposit TEOS for thirty minutes.
4. Epoxy to a thin glass slide. This reduces/eliminates sample rounding.
5. Hand polish the cross section on a "final A" polishing cloth, starting with a 0.25 micron polycrystalline diamond suspension and moving to a 0.05 micron suspension when closer to the fail. This is a lengthy iterative process (polish, look in SEM, polish, look, etc). When in the failing area, a final ion mill to clean the sample and a fluorocarbon-based etch were done to help highlight the sample.

Although a very time consuming, this technique provided clear images of both BOX Opens and Oxide Opens. Figure 11 shows a cross section of an Oxide Open similar to the one in Fig. 3. Figure 12 shows a cross section of BOX Opens which we believe are similar to those in Fig. 7. For this particular wafer, the number of BOX Opens was quite high. Because of the complexity of this FA procedure and the subtleness of the BOX Open defect, verification is still on-going.

This inspection is being used to tune in the DT break-through etch recipe for two different process technologies. While wafers were specially processed with a partial main etch recipe to conduct this work, the cost is not that substantial because the e-beam inspection provided all the information necessary to complete the round of yield learning.

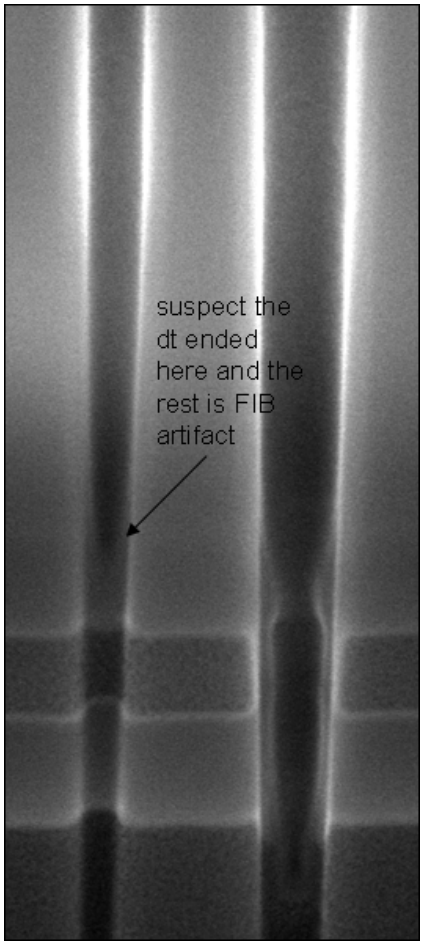

Figure 9: Cross section of bad DT.

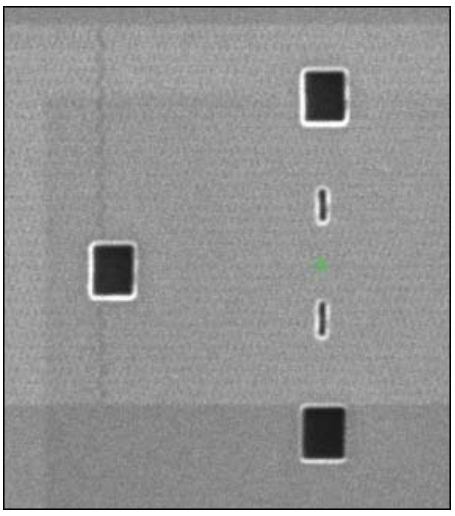

Figure 10: FIB marking for step 2

IV. SUMMARY

Use of VC inspection for optimization of a DT etch process critical to formation of EDRAM capacitors in the substrate of SOI wafers is described. Special processing is necessary to generate a situation where defects can differentiated from good DTs. This special processing is described. Both identification of suitable e-beam conditions for the inspection and FA of the defects were very difficult. The heart of this paper describes this work. This inspection is currently in use for evaluation of etch recipes.

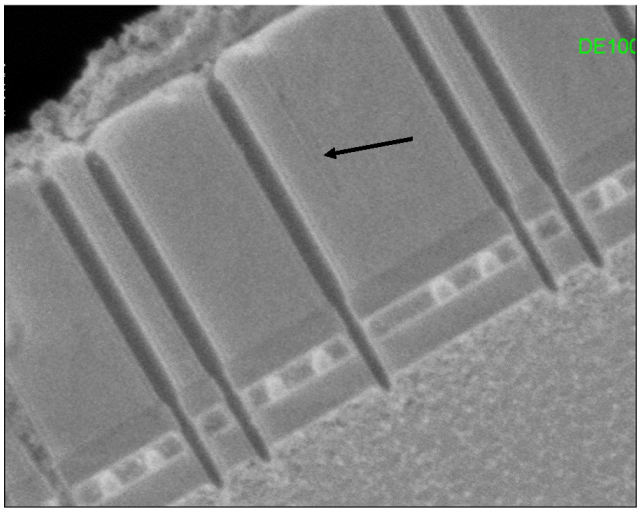

Figure 11: Polished cross section of Oxide Open

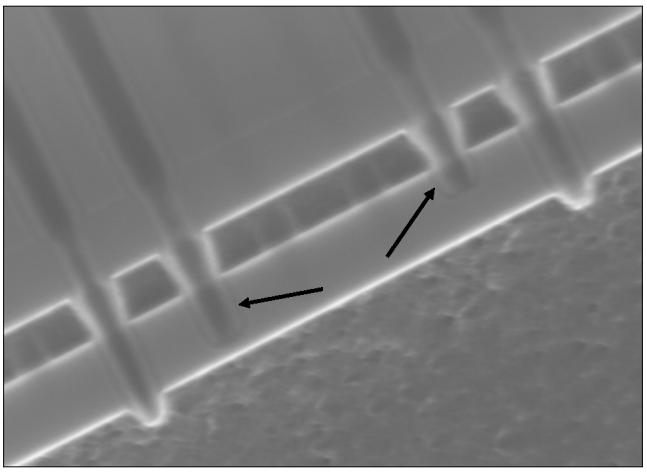

Figure 12: Cross Section of BOX Opens

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