Voltage Contrast Test Structure for Measurement of Mask Misalignment

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Abstract - **A new test structure for measuring mask misalignment for critical levels like contact to gate is described. Alignment requirements have become very challenging because of the extremely small dimensions of current state-of-the-art CMOS devices. The method for measuring contact to gate alignment involves using a SEM to scan an array of contacts each with a different amount of overlap with a grounded gate. The voltage contrast signal indicates which contacts are touching the gate. The data for an example wafer are compared to optical alignment data. Addition work necessary to more thoroughly compare the accuracy of the two techniques is described.**

I. INTRODUCTION

The contact module is possibly the most difficult to implement for new process technologies. Contact size is constrained by the risk of opens if the diameter is too small and the risk of shorting to an adjacent gate if the contact is too large. Contact to gate shorts can be caused by a lot of things besides large contact size including large gate width, physical defects such as protrusions in the gate lines or contacts, and misalignment between the contact and gate masks. Also shorts can occur if multiple of these parameters are marginal. To manage this risk, the variation in these parameters is budgeted to achieve a near zero contact to gate fail rate. Process capability must be developed so that each of these factors reaches its specified target. Then each factor must be controlled to ensure it stays within specification.

This paper focuses on misalignment between the contact mask and the gate mask, which is a very challenging parameter to control. Currently the misalignment between masks is measured optically. As an alternative, we propose a pseudo-electrical technique which uses a voltage contrast (VC) test structure and a SEM capable of seeing VC, such as an inspection SEM. Inspection SEMs are typically used to detect electrically active defects on a wafer [1-3]. Through literature search, we found that a similar structure was proposed 21 years ago prior to the availability of suitable inspection SEMs [4]. Our work shows how such structures can be practically implemented for a modern technology.

In the Section II, the test structure design and analysis procedure are described. Also possible variations of this structure are discussed. In the Section III, data collected for a single wafer are analyzed and compared to optical alignment data. These results show the viability of the technique. The advantages and shortcomings of this VC test structure relative to optical alignment test structures are reviewed. To truly compare the accuracy of this structure versus optical alignment structures, the structures must be laid out next to each other. This and other enhancements planned for the next mask set are discussed.

II. METHODOLOGY

A. Test Structure Design

Figures 1, 2 and 3 show the layout for a VC misalignment test structure to measure contact to gate misalignment. The structure design consists of 80 120nm wide gate lines that are spaced 0.5um apart. These gate lines are grounded to the substrate. A 40nm x 40nm contact is associated with each of the 120nm wide gate lines. These contacts are spaced 0.501um (left two columns) or 0.499um (right two columns) apart, 1nm more or less than the gate line spacing. The result is that each contact is shifted 1nm further up (or down) from its corresponding gate line than its neighbor. The dimensions for this structure are not critical for operation. The designed space between the contact and gate line is indicated for many contacts in Fig. 1. A value of 9 indicates there is a 9nm designed space between the contact and gate line. A value of -5 indicates the contact overlaps with the gate line 5nm. For the left two columns, the contacts are relative to the top edge of the gate line. For the right two columns, the contacts are relative to the bottom edge of the gate line. This two-sided measurement allows both the misalignment and the gate line CD to be measured. If only a one-sided measurement was used, then the effect of misalignment could not be separated from line width variation. The use of two sided measurements is used for electrical test structures in the literature [5]. Figures 2 and 3 are close-ups of small sections of Fig. 1 to show how the contact to gate space changes for each site.

Contacts which physically touch a gate line will become grounded. Under electron beam conditions appropriate for seeing VC, they will light up, indicating they are making contact. Hence, as a set, they indicate the misalignment of the contact to gate mask. In the ideal case where there is not any misalignment and the contact and gate CDs both match design, only the contacts labeled 0 and negative numbers should light up. Figure 4 shows an example inspection SEM image of this structure. This image shows that the gate mask

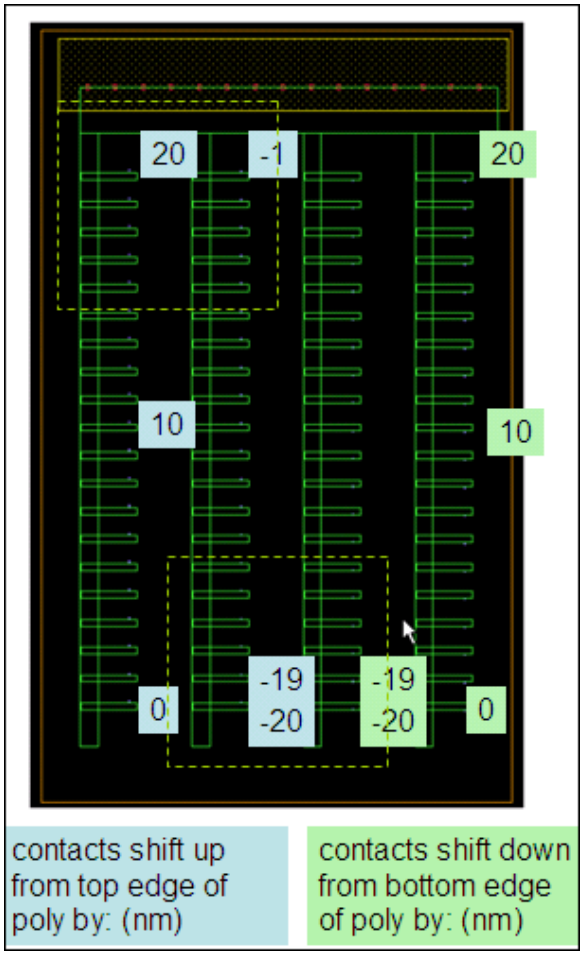

Figure 1: Image of the contact to gate VC test structure design with contact to gate offset labeled. For the left two columns, the contacts are printed on the top side of the gate lines. The offset varies from -20nm to 20nm. At -10, there is 10nm of overlap. On the right two columns, the contacts are printed on the bottom side of the gate lines. The offset varies from -20nm to 20nm

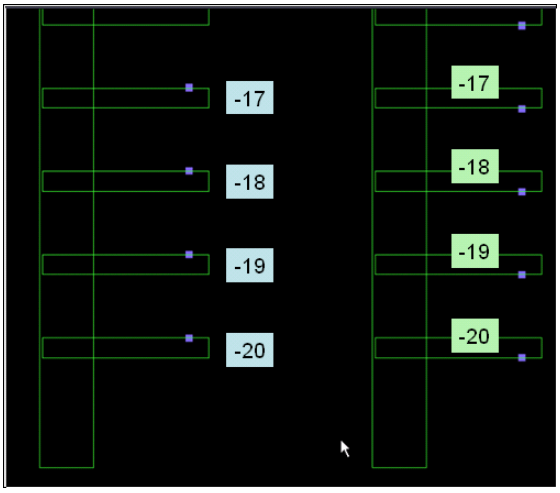

Figure 2: Close-up of the bottom middle dash-bounded region in Fig. 1.

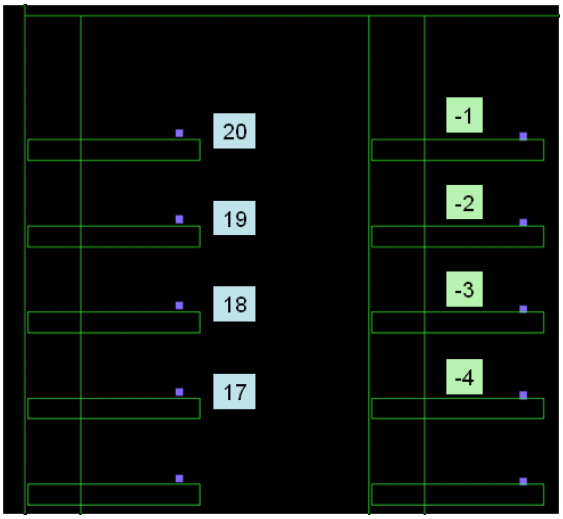

Figure 3: Close-up of the top left dash-bounded region in Fig. 1.

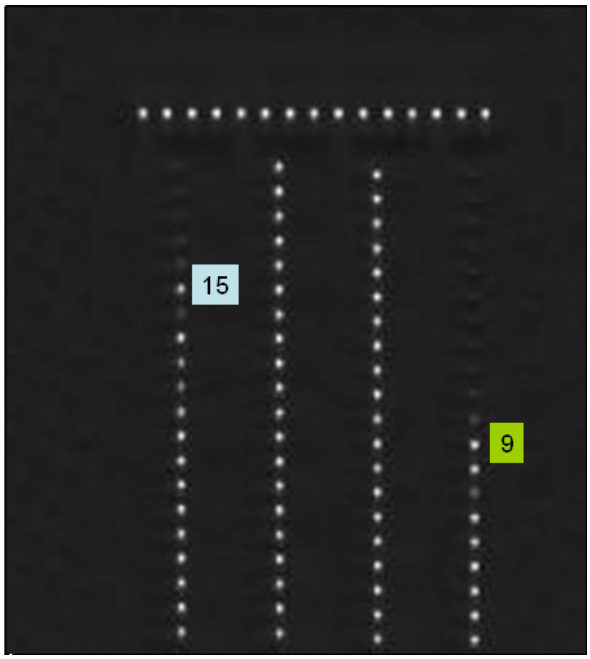

Figure 4: High resolution SEM image of a VC test structure. The contacts are still making contact when shifted +15 up from the designed gate edge and +9 down from the designed gate edge. This indicates the gate mask is shifted 3nm up vs. the contact mask.

is shifted 3nm up relative to the gate mask and that the gate mask is 24nm wider than designed dimension. How these measurements were made will be discussed in the Section IIC.

A key element of the design is the grounding of the gate lines. For bulk technology, this is accomplished using a substrate contact where an active area is doped with P+ S/D but without the standard accompanying N well implant. The result is the P+ S/D region directly contacts the P doped

substrate. The gate-lines are bridged to this grounded active area using rectangular contacts. In Fig. 1, this occurs at the top of the test structure. For SOI technology, IBM's technologies have a mask level to make a hole through the buried oxide. The active area would run over this hole. Again rectangular contacts are used to bridge the gate-lines to this active region. Sometimes it is not possible to make direct contact to the substrate, for instance for short loop wafers. In these situations, a large capacitor may be used as a virtual ground.

B. Apparatus

All the work in this paper was done with a KLA-Tencor eS35 inspection SEM within IBM's E. Fishkill semiconductor fab. Because of the hard grounding, a wide range of electron beam conditions can be used. For this paper, 750V landing energy, 500V Wehnelt voltage, 125nA beam current and 150nm pixel size were selected. A 25nm pixel was used for the high resolution images. Likely even review and CD SEMs using conditions appropriate to see VC can be used to evaluate these structures. The VC alignment test structures shown in this paper were implemented on a 28nm bulk mask set, although similar structures have been implemented for 45, 32 and 22nm SOI and bulk technologies. This technology is a 90% shrink of the 32nm bulk technology, so the test structure dimensions are actually 90% of the designed dimensions listed above. For simplicity, we will present the analysis in terms of designed dimensions also.

C. Procedure

These structures are monitored with an inspection SEM using the following procedure:

1. Image collection – Use low values for inspection threshold and merge distance so that a single, giant defect covering the entire care area is "detected" for each site. This results in a single centered image of each instance of the test structure. Random mode inspection is necessary. A high resolution image capture step is included to get the best possible quality images.
2. Count bright contacts – Count the number of bright contacts from the 1nm and larger sites in Fig. 1 for the left two columns (L) and the right two columns (R). They should be consecutive, but if a single contact is dark in the midst of bright contacts, ignore it. If none are bright, then record the number of the largest bright site.
3. Calculate the misalignment – Take the difference between the bright contacts on the left and those on the right and divide by 2. This indicates the misalignment of the gate line in the Y direction relative to the contacts (M). If M is negative, this indicates the gate mask is shifted in the negative Y direction.

$$M = (L - R)/2 \quad (1)$$

4. Calculate the gate linewidth delta from design dimension (dLW_P) –The sum of L and R is due to variation in the gate and contact CD from nominal. To separate out, it is necessary to drawn on the final CA measurement from a CD SEM (dLW_C), which typically is available.

$$dLW_P = (L + R) - dLW_C \quad (2)$$

For instance, in Fig. 2, L is 15 and R is 9. Assume the measured contact CD is 40nm which matches the designed CD. Then dLWc is 0. From Equations 1 and 2, M is 3nm and dLWp is 24nm. Since the gate lines were designed at 120nm, the gate line for this structure is 144nm.

If this test structure proves to be superior or at least complementary to optical alignment test structures, then special data analysis software and even a special SEM tool will eventually be developed to handle these calculations. This tool would output wafer maps with the exact misalignment and line width values.

D. Design Variations

Many different variations of this structure are possible. Two obvious ones are to change the mask levels and orientation. Figure 5 shows a set of VC alignment structures that was included on a 28nm bulk technology mask set. This technology currently uses dual patterning for the contact module. The contact levels are called CA and CB. Figure 5 includes structures for CA to gate, CB to gate, CA to active, CB to active and Metal 1 to CA alignment. The lower mask level must be grounded as only the upper mask level can be measured for a VC signal. For instance the CA level must be grounded for the metal 1 to CA alignment structure. Each of these structures is drawn in 0^o and 90^o orientations to monitor the misalignment in both directions. Note that for today's cutting edge technologies, pattern fidelity is better in one orientation than in the other for certain mask levels. For contact to gate misalignment, the Y direction is much more important than in the X direction because the gate lines of the SRAM cell flow horizontally. For logic, the gate lines can also run vertically but the dimensions are relaxed.

Because all contacts physically below a particular contact in the structure have more overlap by design, if a contact is bright, its neighbors below should be expected to be bright also. This is not always true. See for instance Fig. 4 where the 2^{nd} contact from the top bright one in the left column is dark. The primarily cause is believed to be line edge roughness and CD variation on both the gate and contact features. To account for this effect, multiple replicates of the same alignment structure may be included or multiple contacts could be included for each gate line as shown in Fig. 6. More recent IBM mask sets include the former but future ones will include the latter because of greater simplicity in data analysis.

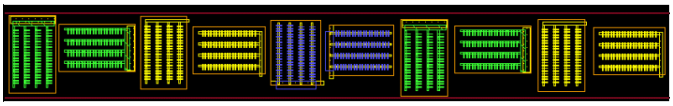

Figure 5: VC alignment structures on a 28nm bulk mask set. They include contact to metal 1 (blue), contact to active (yellow) and contact to gate (green).

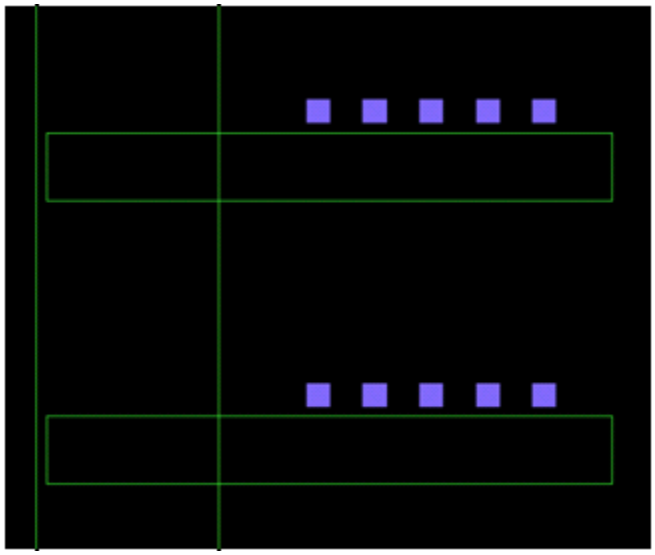

Figure 6: Potential contact to gate alignment structure design with multiple contacts to eliminate noise and measure line roughness

III. EXPERIMENTAL

A. Results

The VC alignment test structure measurements were compared to optical alignment measurements for a 28nm wafer after WCMP. Figures 7 and 8 show dLWp and M for this wafer. For all sites the gate mask is shifted in the positive Y direction by values varying from 0 to 7.5nm. The wafer has pattern. The dLWp wafer map shows the gate is wider in the center of the wafer. This is consistent with optical measurements. For simplicity, we assumed the contact CD is right on target. An accurate gate line width measurement was not the primary focus of this work.

Measurements from optical alignment structures were used to judge the accuracy of the VC alignment structure. Optical alignment structures are located throughout the reticle field. A special recipe was created to measure a number of sites near the VC alignment structure for all full die on the wafer. Figure 9 shows the location of these and the VC measurement site on a die map. Four of the measurements included are at the corners of the reticle field which is approximately 26mm x 33mm. Figure 10 shows the optical measurements across the wafer for the nearest site. The match between the VC and optical alignment structures is good, but is far from perfect. For instance, for both the left side of the wafer has the least misalignment and the right side has the most. Figure 11 is a scatter plot comparing the VC and the optical measurements for the closest site. The measurements have a strong correlation but there is a lot of noise. This is partly because the misalignment varies a great deal across the reticle field. Figure 12 shows the four closest optical measurements and the VC measurement for each die. The X axis is ordered by column.row of the die. This plot shows that the optical values vary a lot even though they are very close together. The average spread is 1.3nm for the optical structures. The VC measurement is often at the top end of this range. Remember, these measurement points are all within 5.3mm of each other whereas the VC alignment structure is 6mm away from all but the closest point. Because of the impact of location on the reticle, it is difficult to evaluate the accuracy of the VC misalignment structure further by comparison with optical measurements. A new VC alignment structure macro design is necessary where VC and optical misalignment structures are placed right next to each other.

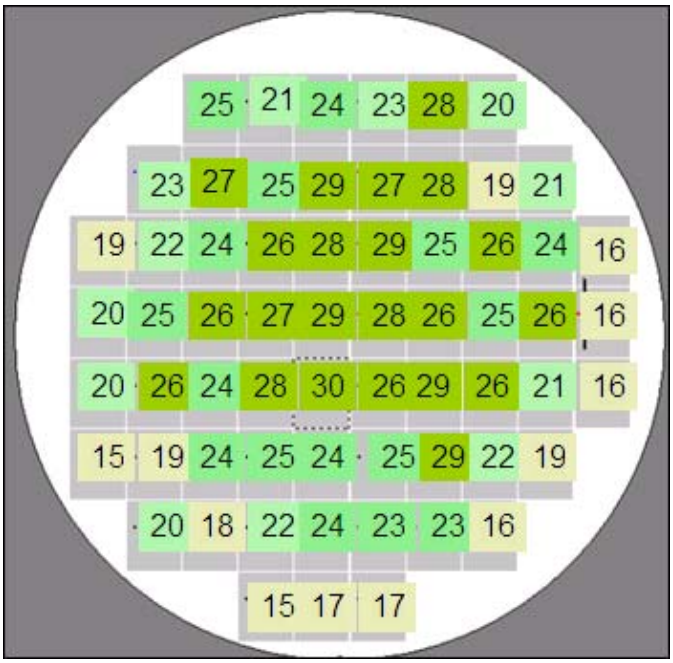

Figure 7: Gate line width delta (dLWp) from the VC test structure

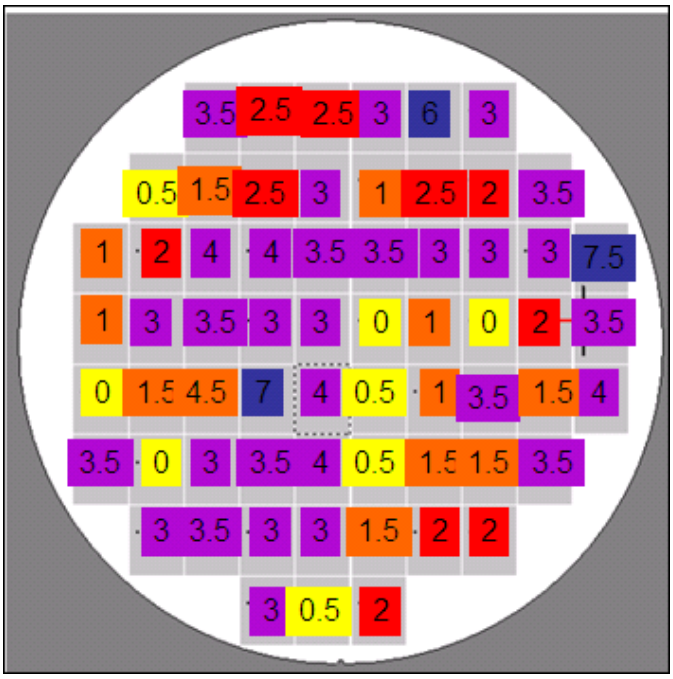

Figure 8: Contact to gate misalignment measured by VC test structure. The numbers represent the gate shift in the Y direction relative to the contact mask. For all die, the shift is positive and varies from 0 to 7.5.

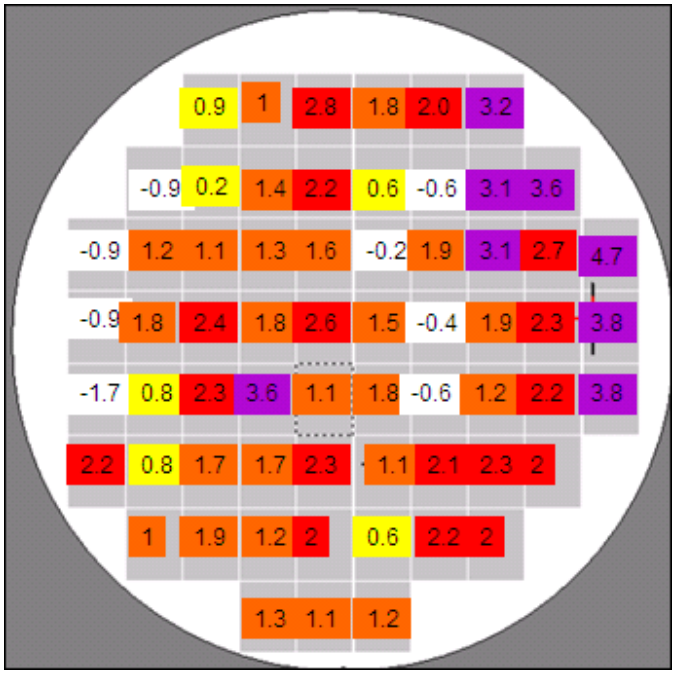

Figure 10: Optical misalignment measurement data. The general trend across the wafer matches Fig. 7.

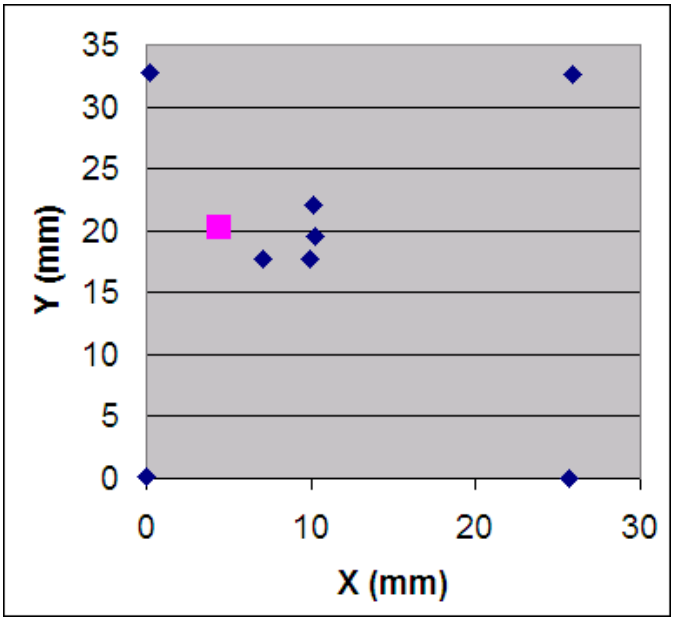

Figure 9: Location of VC and optical alignment structures on the reticle field. Square – VC measurement site. Diamonds – optical measurement sites.

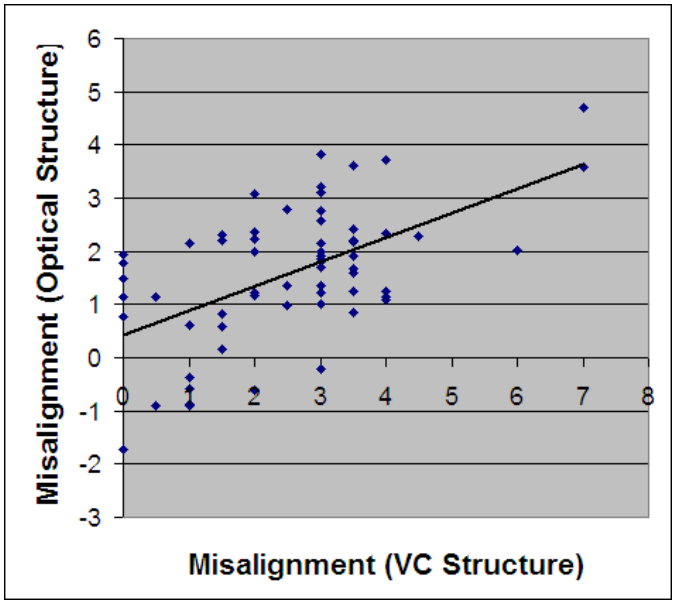

Figure 11: Scatter plot of misalignment data from VC and optical test structures. The measurements correlate but there is a lot of noise.

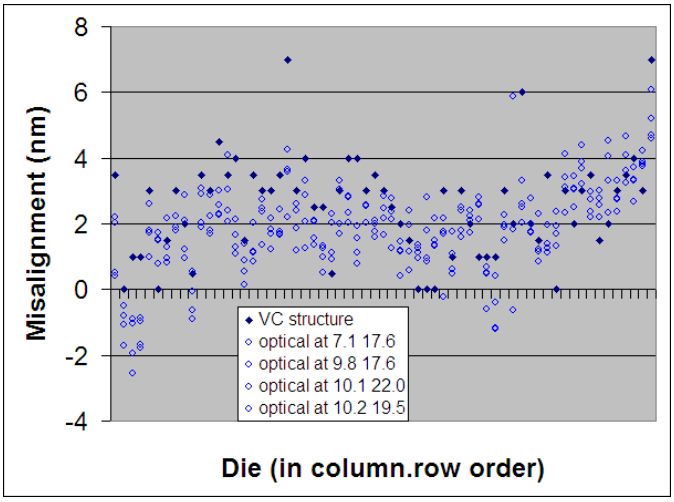

Figure 12: Misalignment from the four nearest optical measurements sites and the VC misalignment measurement site vs. die

B. Comparison to Optical Measurement for Practical Use

This VC misalignment measurement technique has both advantages and disadvantages vs optical measurement. Also there are similarities. Just like the optical technique, VC measurement is made at level. The small size of the structure allows placement at multiple locations across the reticle field just like the optical structures. The VC structure cannot however be used to measure photoresist and therefore would not be useful for the photo rework loop. On the other hand, this technique is potentially more accurate and may use the exact feature dimensions of importance. Also because gate, contact and other features are not 2-dimensional, the VC technique captures the impact in the Z direction better. Figure 13 shows a TEM cross section of the alignment test structure. The right contact is 1nm closer than the left contact but neither is making contact with the gate. Both the contacts and the gates have a slope. Although from the top down perspective, they may intersect, because the contact gets narrower at the bottom, they very well may not intersect. Therefore the VC structure gives a better sense of the process window.

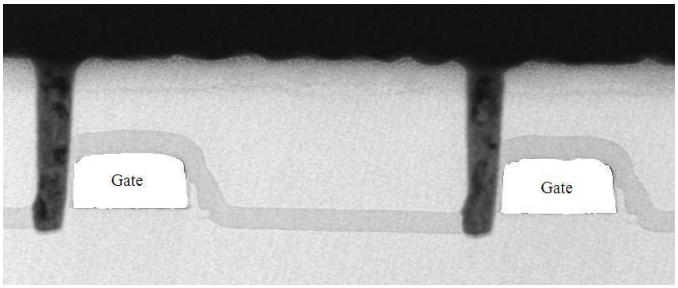

Figure 13: TEM cross section of a VC misalignment structure.

C. Future Designs

While the structures on this mask set have been sufficient to establish that this is a viable technique for measuring mask alignment, a new set of structures is necessary to evaluate the accuracy relative to optical alignment structures. For the next round of structures, these are the enhancements that will be made:

- Optical alignment structures will be placed right next to the VC alignment structures.
- The VC structures will contain multiple contacts, as in Fig. 6, to average out noise and get a sense of line edge roughness.
- There will be more space between structures so that the edge of next one is not captured in the image. This might make image processing easier.
- A smaller step size will be used. For 28nm bulk technology a 1nm step size was used. For the next design a 0.25nm step might be used.
- The structures will be placed on multiple locations around the reticle field.
- Confirm OPC does not alter the structures from their intent. OPC could potentially alter the CA or PC shape giving misleading results.

IV. SUMMARY

A test structure for measuring mask misalignment electrically using an inspection SEM was described. Elements in the lower layer are grounded and elements in the upper layer are floating and are offset from the lower elements in increasing steps. Those that make contact with the lower layer elements become grounded, which is detected by an inspection SEM. The number of grounded elements is used to calculate the misalignment. The feasibility of this VC test structure was demonstrated. The misalignment measurements were comparable to those from optical alignment structures. Planned modifications to the VC alignment structures for better comparison with optical alignment structures were described.

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