Patterned Wafer Geometry Grouping for Improved Overlay Control

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ABSTRACT

Process-induced overlay errors from outside the litho cell have become a significant contributor to the overlay error budget including non-uniform wafer stress. Previous studies have shown the correlation between process-induced stress and overlay and the opportunity for improvement in process control, including the use of patterned wafer geometry (PWG) metrology to reduce stress-induced overlay signatures. Key challenges of volume semiconductor manufacturing are how to improve not only the magnitude of these signatures, but also the wafer to wafer variability. This work involves a novel technique of using PWG metrology to provide improved litho-control by wafer-level grouping based on incoming process induced overlay, relevant for both 3D NAND and DRAM. Examples shown in this study are from 19 nm DRAM manufacturing.

Keywords: Overlay, wafer shape, wafer stress, patterned wafer geometry.

1. INTRODUCTION

As ground rules shrink, advanced technology nodes in semiconductor manufacturing demand smaller process margins and hence require improved process control. Overlay control has become one of the most critical parameters due to the shrinking tolerances and strong correlation to yield. Process-induced overlay errors, from outside the litho cell, including non-uniform wafer stress, has become a significant contributor to the error budget. Previous studies have shown the correlation between process-induced stress and overlay and the opportunity for improvement in process control [1, 2]. Patterned wafer geometry (PWG) metrology has been used to reduce stress-induced overlay signatures by monitoring and improving non-litho process steps or by compensation for these signatures by feed forward corrections to the litho cell [3,4]. Of paramount importance for volume semiconductor manufacturing is how to improve the magnitude of these signatures, and the wafer to wafer variability. Standard advanced process control (APC) techniques provide a single set of control parameters for all wafers in a lot, and thereby only provide aggregate corrections on a per chuck basis. This work involves a novel technique of using PWG metrology to provide improved litho-control by wafer-level grouping based on incoming process induced overlay.

Wafer stress induced overlay is becoming a major challenge in semiconductor manufacturing, and the percentage contribution to the overlay budget is increasing. Addressing non-litho overlay is paramount to reducing wafer level variability. The amplitude of stress and the overlay budget differ by market segment. We observe from Figure 1 that the 3D NAND, for example, has the largest magnitude of wafer shape induced stress, but also has a relatively large overlay budget of 8 to 20 nm. DRAM, on the other hand, has less stress, but has a much tighter overlay spec of 2 to 3 nm. The relative stress level and overlay budget dictate different process control use cases. For the case of 3D NAND, the improved overlay can be achieved using the PWG stress data for process monitoring as mentioned earlier, or by directly providing the stress based feed forward corrections to the litho cell [3, 4]. In this work, we will focus on the DRAM device application. Key topics include identifying process signatures in the shape data, and using those signatures to reduce within lot variability.

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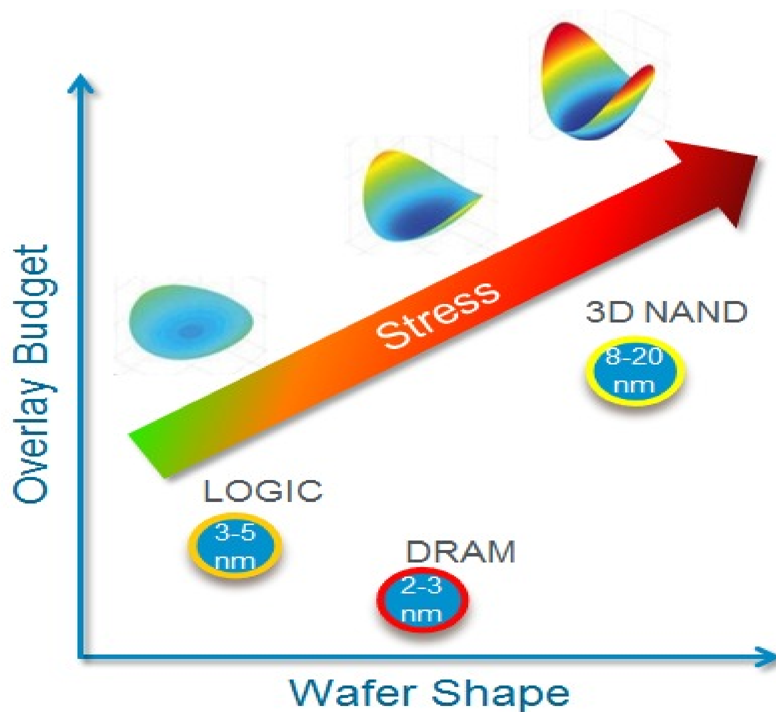

Figure 1: Wafer shape vs. overlay budget for advanced semiconductor processing. Each major technology sector (logic, DRAM, and 3D NAND) has different levels of stress and different overlay budgets.

Firstly, we will discuss the connection between wafer shape and overlay. During integrated circuit manufacturing many layers are printed on a silicon wafer. There is a critical need to align precisely pattern layers to an underlying pattern. This requirement is often complicated by process induced stress variations distorting the under-layer pattern, as illustrated in Figure 2 [5, 6]. A reference layer pattern is formed at a certain level N (or layer N) and the pattern is initially defined by the characteristic length L shown. To form level N+1, a film is first deposited on top of level N. Film stress causes the wafer to warp in free-state resulting in a change to shape of wafer. This is typically manifested as both out-of-plane displacement (OPD) and in-plane displacement (IPD), affecting lateral placement of the under-layer pattern (level N). To print the level N+1 pattern the wafer is forced flat (e.g. lithography vacuum chucked). For the most part, chucking the wafer fully reverses the out-of-plane displacement but the in-plane displacement is only partially reversed. Thus the under-layer pattern is now displaced relative to where it was originally printed. If level N+1 pattern is printed without correcting for the under-layer distortion, it results in misalignment or overlay error between the two layers. Such an overlay error is known as process-induced or process-stress induced overlay error and it can be caused by any type of stress inducing semiconductor process such as film deposition, thermal anneal, etch, CMP, etc.

Wafer shape is measured by a unique implementation of a dual-Fizeau interferometer on KLA-Tencor Corporation's WaferSight™ PWG patterned wafer geometry and nanotopography metrology system [7]. Simultaneous back side and front side measurements are made with the wafer in a vertical orientation to eliminate gravitational distortion. Overlay is measured on a KLA-Tencor Corporation Archer™ 500 overlay metrology system using Archer AIM® optical imaging metrology targets.

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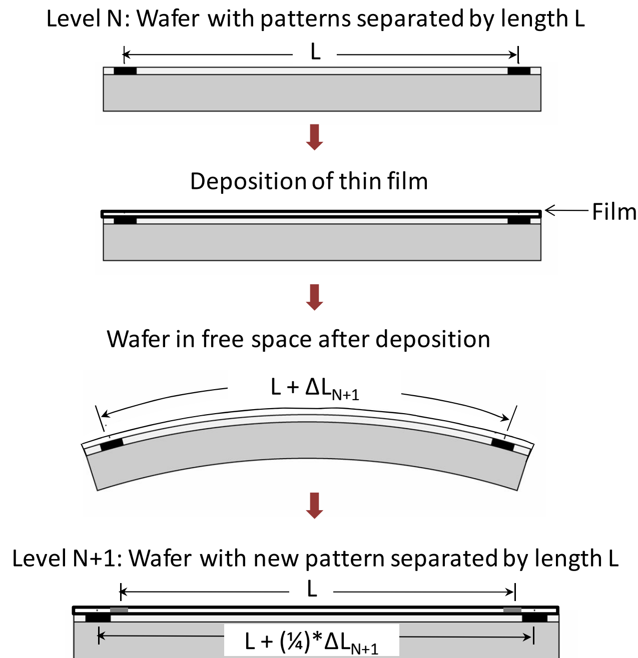

Figure 2: Illustration of the effect of film stress on wafer shape leading to overlay errors [6]

It has been shown that process-induced overlay error can be accurately estimated from the change in shape induced by semiconductor processes [2, 6, 8, 9]. Figure 3 shows a simplified schematic of a semiconductor process flow of a single layer. To estimate potential overlay error induced by processes between the reference lithography step (e.g. level N) and the current lithography step (e.g. level N+1), it is necessary to make wafer geometry measurement at the two indicated points in the figure as "pre" and "post", corresponding to before and after the shape or stress inducing process steps. Once wafer geometry measurements become available, the change in the shape induced by processing is calculated as the difference between two measurements. Process-induced overlay error can then be calculated from the shape change by using one of several algorithms that have been developed [2, 6, 8, 9]. In this paper, we use an advanced IPD algorithm based on two-dimensional plate mechanics for the accurate estimation of the process-induced overlay error referred to as GEN3 [2].

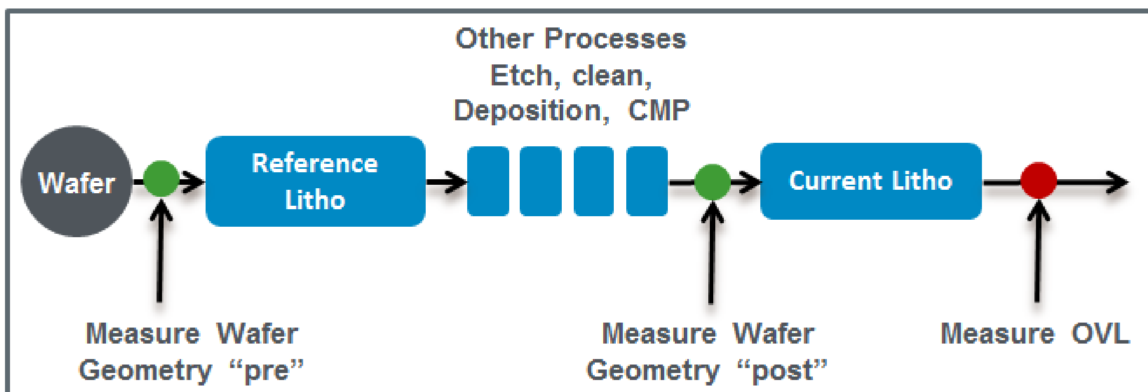

Figure 3: Metrology and processing sequence used for this investigation: Pre- and post-wafer geometry metrology, and post-litho overlay metrology.

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2. SHAPE BASED OVERLAY FOR DRAM

As discussed previously, different semiconductor processes have varying levels of stress and different overlay error budgets, including 3D NAND, DRAM, logic, etc. These differences require different process control use cases, such as feedback, feed forward, grouping, etc., alone or in combination. In this work we describe an advanced grouping process control use case for DRAM in order to minimize overlay. For this investigation we look at a specific implementation of wafer grouping which is appropriate to R&D environments and ramp-up of high volume manufacturing (HVM) called here send-ahead grouping (SG). The more general grouping use case for HVM will be addressed in a future report.

In order to meet the tight overlay specifications for the next generation DRAM devices, a send-ahead grouping (SG) based on the shape data has been evaluated. The flow of the proposed SG is outlined in Figure 4. Firstly, all the wafers in a lot are measured with a PWG tool for both "pre" and "post" layers. The shape data from the difference of these measurements is then used in the GEN3 algorithm to determine stress or shape based predicted overlay. The wafers are then grouped by similarity of wafer signatures. Grouping optimization is performed using the predicted overlay after removing the POR scanner alignment model. The grouping optimization: (i) decides the optimal number of process signatures; (ii) identifies the process signatures; and, (iii) provides a list of recommended wafers for metrology and exposure (step 2 in Figure 4). The selected wafers are then exposed by the scanner in step 3 and the overlay measurement is performed in step 4. Finally, the correctable coefficients for each group will be calculated separately using the overlay metrology data. The exposed wafers will be reworked and then the entire lot will be exposed using the group by group corrections.

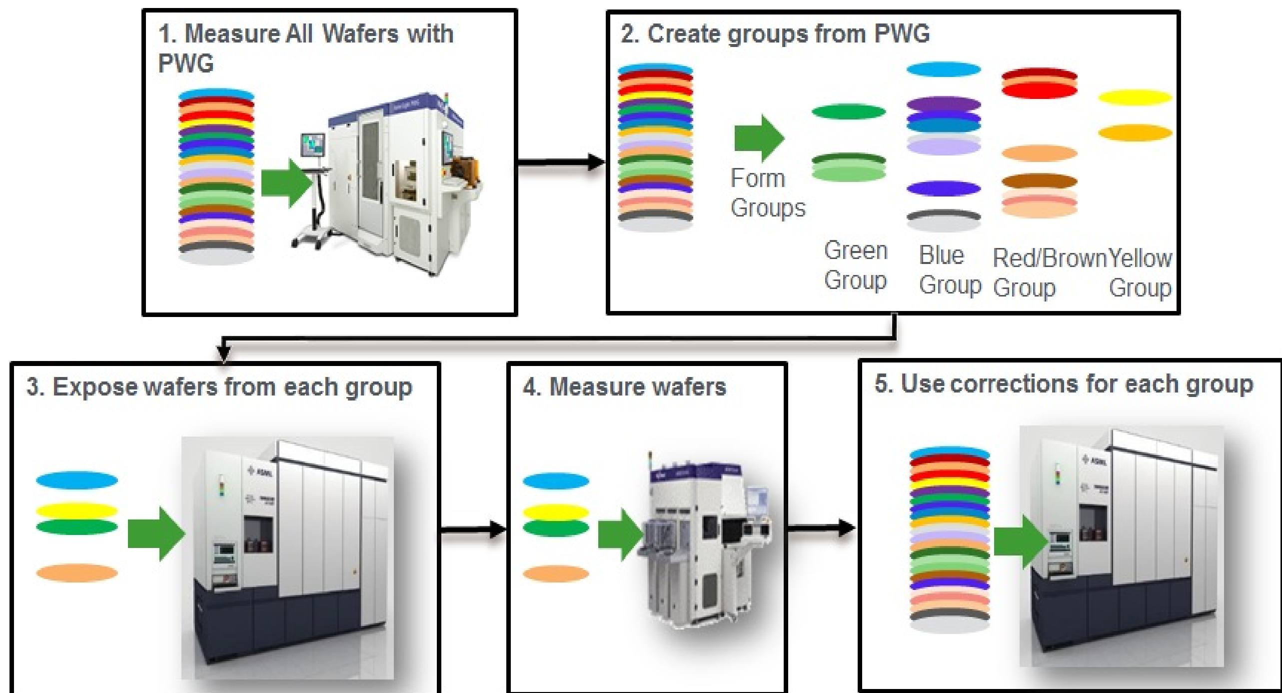

Figure 4: Shape based overlay control grouping use case for DRAM R&D and process ramp.

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3. WITHIN LOT VARIABILITY

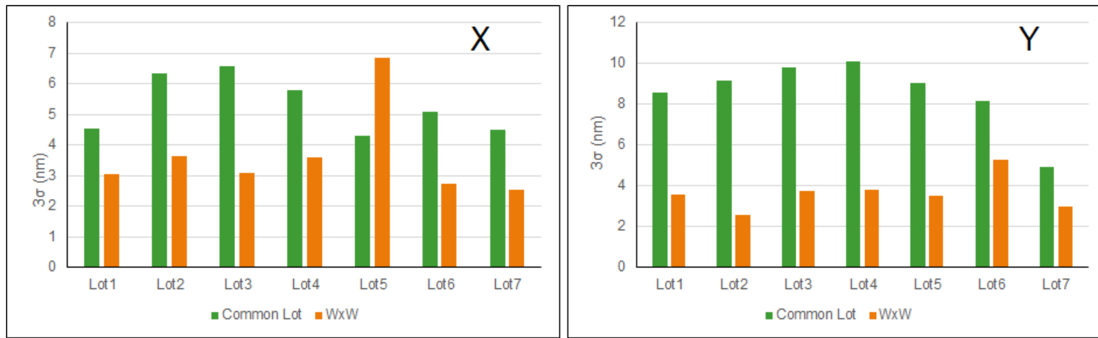

Figure 5: Overlay budget breakdown analysis by a rigorous ANOVA to quantify wafer-by-wafer variability: 3σ in nm for X and Y directions.

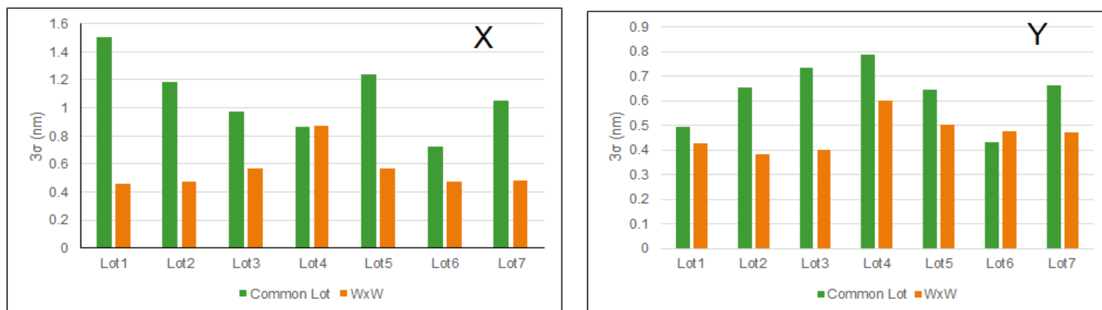

Figure 6: Budget Breakdown Analysis of the predicted overlay using wafer shape data: 3σ in nm for X and Y directions.

The work is aimed at reducing the within lot variability. The within lot variability or wafer by wafer (WxW) variability is becoming one of the most important challenges to achieve tight overlay specifications for next generation DRAM devices. First we quantify within lot variability for both the shape and the overlay data using a rigorous analysis of variance (ANOVA). We analyzed seven lots individually and the results for both the overlay and PWG data are presented in Figures 5 and 6 respectively. The overlay data show an average of 3.6 nm WxW variation in both the X and Y direction. The shape based overlay average within lot variation is 0.55 nm in X and 0.46 nm in the Y direction.

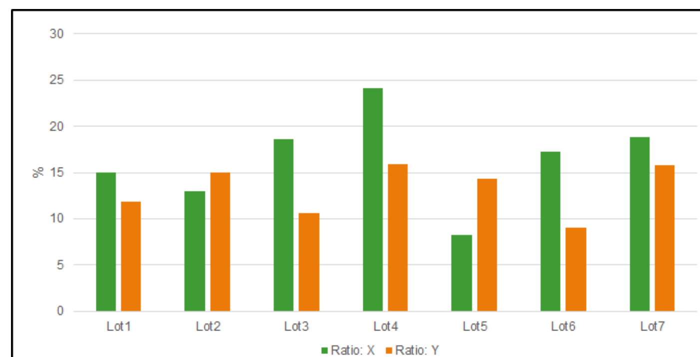

Figure 7: Ratio % of the shape WxW variability to the total overlay WxW variability by lot for X and Y.

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It should be noted that the within lot variation of the overlay data is comprised of different sources and the shape based overlay explains only part of the total within lot overlay variation. Figure 7 shows the ratio % of the within lot variation shape based overlay versus the total overlay for both the X and Y direction. It can be seen that shape overlay can explain as much as up to 25% of the total overlay variability. These findings indicate that minimizing the impact of stress based overlay, from processes outside the litho cell, will provide potentially significant improvement, which is critical in the drive towards 2 nm overlay.

4. DRAM CLUSTERING RESULTS

For all of the analyses presented in this study, the GEN3 algorithm was used to calculate stress based overlay. To perform grouping the scanner alignment model was first removed from the stress based overlay for each wafer. The alignment removes some of the within lot variations, however, wafer level alignment is not sufficient to remove all the wafer level variations. One useful way to visualize data variation is by performing Principle Component Analysis (PCA) of the data. By performing PCA, we express data in terms of Eigen functions of the covariance matrix of the data. Eigen values of the covariance matrix are calculated such that the first principle component explains the largest variation of the data, the second explains the second largest variation and so on. The coefficient for each principle component (PC) is referred to as the score. Figure 8 shows scores for the PC1 (first principle component) versus the PC2 (second principle component) for all the wafers for a single lot using stress based overlay. Two distinct groups, indicating two distinct process signatures can clearly be observed in this lot.

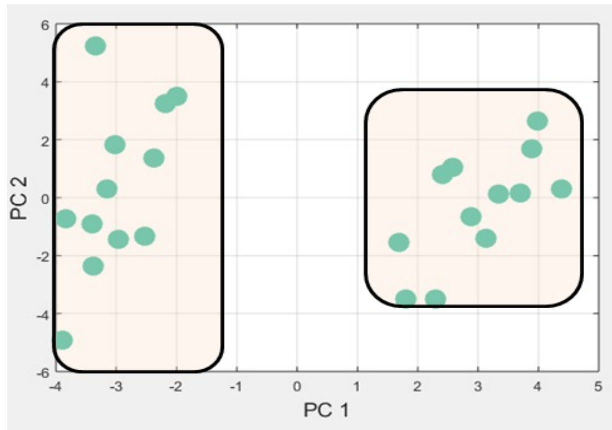

Figure 8: Identification of shape signatures based on PCA: two populations are clearly visible.

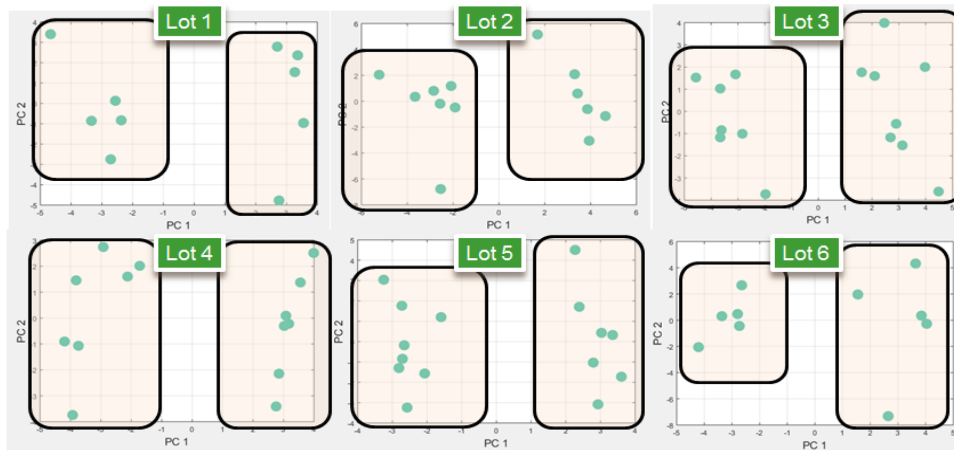

Figure 9: PCA analysis for the other lots. Shape data successfully captures the process context.

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The same analysis was performed for the rest of the six lots as shown in Figure 9. For all the lots in this example, two signatures can clearly be observed in their leading scores plot. Some excursion wafers were removed from the analysis. After observing these clear process signature groupings, it was confirmed that the signatures correspond to the two stages of a process tool. This clearly proves that the stress overlay grouping method can successfully identify and distinguish significant process signatures. It should be noted that in the general case the optimal number of groups would not necessarily be two.

We quantified the stress overlay grouping by performing comprehensive send-ahead grouping (SG) simulation study. Grouping optimization was performed using the shape data to select optimal number of groups and also the send-ahead wafers for processing and metrology. Then using the send-ahead wafers for each group, ideal corrections were simulated and applied to each group in the lot. From the composite group residual, |mean|+3σ for each wafer was recorded. The residual |mean|+3σ was also calculated using the standard plan of record (POR) wafers. The root mean square for the average of the |mean|+3σ for X and Y is compared between SG and POR in Figure 10. The average |mean|+3σ improved by more than 0.5 nm using the SG solution.

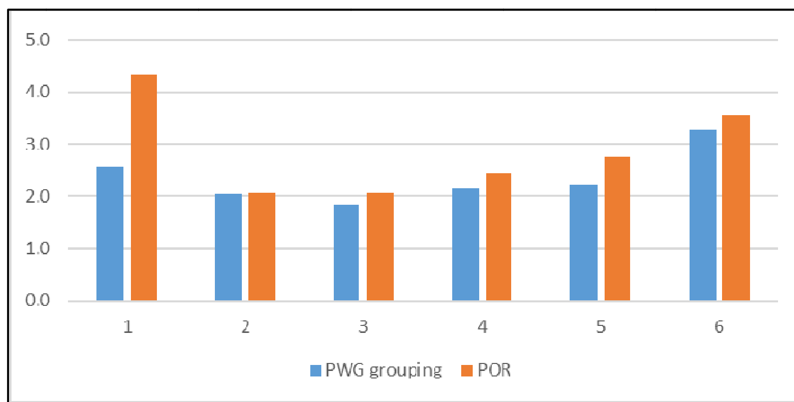

Figure 10: Improvement of wafer-by-wafer variability: average of |mean| + 3s by lot resulting in > 0.5 nm average improvement.

The range is defined as the difference of the maximum and minimum |mean|+3σ per lot for both the X and Y direction. Figure 11 shows the comparison of the RMS of X and Y ranges for the six lots. The range has been improved by about 1 nm, underscoring the benefit of controlling wafer level variation by using shape data to identify signatures and group wafers for exposure and metrology.

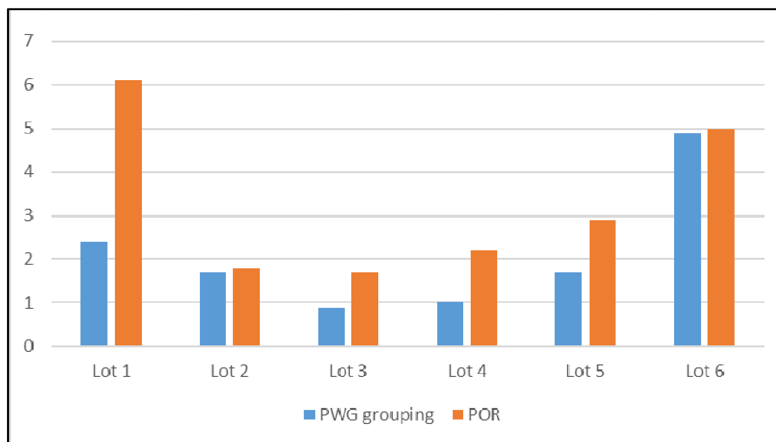

Figure 11: Improvement of wafer-by-wafer variability: range of |mean| + 3s by lot resulting in > 1.0 nm range improvement.

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5. CONCLUSIONS

Process induced overlay errors from outside the litho cell have become a significant contributor to the overlay error budget. It is no longer sufficient to focus exclusively on litho cell overlay improvement. Addressing non-litho overlay is key to reducing wafer level variability. We demonstrated a novel technique of using PWG metrology to provide improved litho control by wafer-level grouping based on incoming process induced overlay in a 19 nm DRAM manufacturing process driving towards a 2 nm overlay budget. Wafer to wafer variability range was reduced by around 1 nm across the lots in this study. Future directions include a full HVM implementation of the grouping methodology.

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