# Detection of Printable EUV Mask Absorber Defects and Defect Adders by Full Chip Optical Inspection of EUV Patterned Wafers

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***Abstract*— The ability to rapidly detect both printable EUV mask adder defects as well as mask absorber defects across the entire mask image field is a key enabler for EUV lithography. Current optical wafer-based inspection techniques are only capable of detecting repeater defects on a Die-to-Die basis for chiplets within the image field. Larger server-type chips that encompass the entire mask image field cannot rely on such a scheme, since the presence of the defect in every die prevents their detection. In this study, a prototype optical wafer defect inspection methodology designed to detect repeater defects over the entire image field, termed Die-to-Baseline Reference Die (D2BRD), is investigated. The sensitivity of this inspection technique is demonstrated and compared to eBeam inspection over a range of defect sizes for both opaque and clear type mask absorber programmed defects. Moreover, the D2BRD methodology is used to monitor printing defect adders present in a lithographic defect test mask, as well as 7 nm metal mask layer. Using defect repeater analysis, SEM review and patch image classification of full chip wafer inspections over several mask cycles, the D2BRD scheme is shown to allow the unambiguous identification of both mask adder and absorber "native" mask defects, while suppressing random process defects. Thus, this methodology has the potential to help define the risk assessment of mask adder defects in the absence of an EUV pellicle, and can play an integral part of the wafer print protection strategy.**

***Keywords—EUV, defects, inspection, mask, adder***

## I. INTRODUCTION

A key challenge for introduction of EUV to production fabs is to ensure that defects that land on the mask preferably not print on the wafer. The introduction of an EUV pellicle will limit this threat, but will not guarantee that printable wafer defects will not occur due to mask defect adder events. To circumvent this limitation, an inspection technique that allows us to detect EUV mask printable repeater defects present on the entire product chip is required for successful implementation of EUV. From an inspection standpoint, large server chips that encompass the entire image field cannot rely on a Die-to-Die (D2D) detection strategy for the identification of repeater defects, since their presence in every die precludes their detection. Die-to-database eBeam inspections have the necessary resolution for adder detection [1-2] but, currently lack the throughput to be used for regular monitoring of full chips. An optical inspection solution with sufficient detection sensitivity that can identify repeater defects in both logic and array regions of the entire die in a high throughput manner would thus be ideal.

We have previously characterized an optical inspection methodology termed 'Die-to-Baseline Reference Die', (D2BRD), in which repeater detection is achieved by comparison of the test die image with a 'golden' recorded reference image [3]. The technique, which includes algorithms that allow suppression of random process defects, was shown to be capable of identifying both clear and opaque mask absorber programmed defects down to the limit of defect printability threshold. In this work, we go beyond detection sensitivity characterization and demonstrate how full-die D2BRD inspection can be used to monitor printing new repeater defects present in test monitor masks as well as product masks. Thus, the technique has the potential to become an integral part of a strategy to monitor health of EUV masks.

## II. METHODOLOGY

As mentioned above, in a D2BRD methodology, EUV mask defect detection is achieved by comparing a wafer exposed with a mask that has a number of use cycles, to a 'golden' reference wafer, exposed with the mask at a baseline time, '$T_0$'. This is accomplished using a Broad-Band-Plasma (BBP) patterned wafer inspection tool typically used for process-induced defect detection, but with a commercial prototype implementation of D2BRD termed Standard Reference Die (SRD). A more detailed view of the methodology is shown

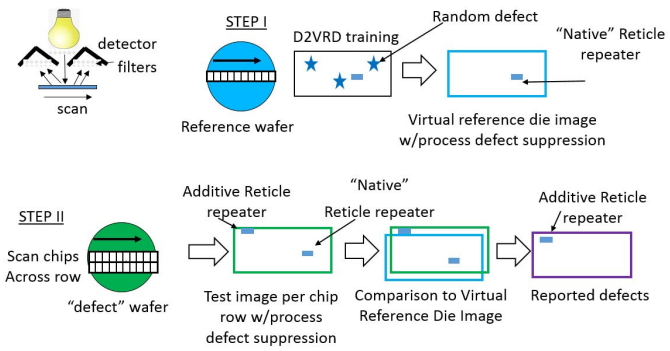


Fig. 1. D2BRD Methodology: Step 1 shows that a single die row is scanned to create pixel map of a composite die reference. Step 2 shows that for each scanned row a composite die image is compared to the virtual reference die in order to extract the mask defect adders

schematically in Figure 1.
In Step I the D2BRD recipe is created in a similar fashion as a regular inspection. In this case, however, recipe creation includes the recording of a composite reference single die pixel map generated by averaging all dies in a row. The averaging of all dies allows repeater defects of an intensity greater than a given threshold to be included in the golden reference, while effectively suppressing random process defects. In Step II, the test wafer will be scanned and, once again, each die in a row will be combined to create a composite image for that die-row. Defect detection will be accomplished by a pixel-by-pixel comparison of the test composite die-row image with the stored golden reference. Consequently, it is expected that random process defects, as well as inherent mask defects present in both reference and test composite dies, will not be detected with this methodology; only mask repeater adders should be detected by D2BRD.

The test mask used in this work has been previously described [2-3], and contains programmed defects blocks with various clear and opaque defect types in horizontal and vertical 1:1 line/space patterns at a range of pitches. A reference block contains the same pattern without the defect, and is used to create the golden composite reference die image. The sensitivity of the inspection methodology is characterized with defects types that vary incrementally in size by 4 nm (4x at mask dimension) from a maximum design size of 120 nm in one orientation. In addition, the test mask contains large repeating arrays of 1:1 line/space horizontal and vertical patterns used for defectivity assessment.
The study also contains mask adder repeater detection results from one of our 7 nm node Metal 1 level EUV product masks. To achieve full-die inspection for the M1 mask at high sensitivity and with low nuisance rate, a strategy for care area generation that differs from the conventional device-centric strategy was developed, as described in section V.

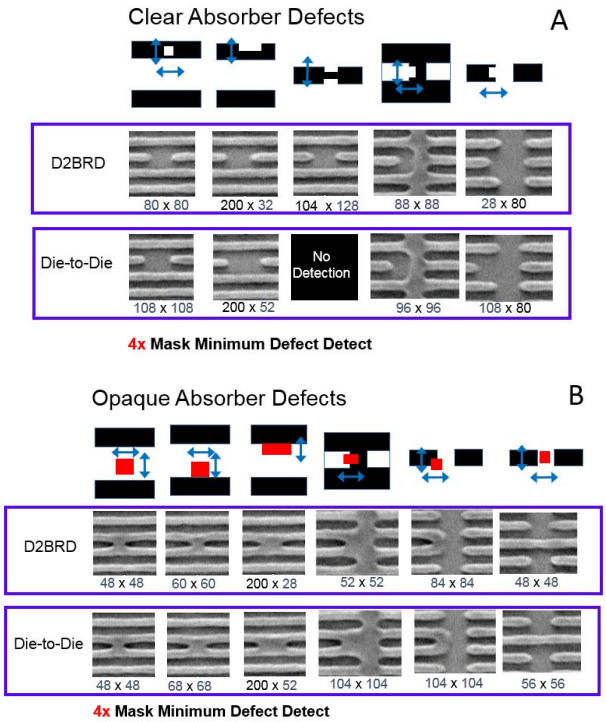


Fig. 2. Comparison between the D2BRD and D2D programmed defects sensitivity for (A) clear absorber mask defects and, (B) opaque absorber mask defects. SEM images of the minimum detect size, displayed with 4x mask defect design sizes are shown.

## III. Sensitivity of D2BRD Inspection: Programmed Defect Studies

The programmed defects in our test mask were a convenient vehicle to characterize the sensitivity of the D2BRD methodology, and to gauge the actual size of the defects being printed per defect type. Figure 2 shows representative images of a few of the programmed defect designs, corresponding to both clear and opaque type of defects in the absorber, overlaid onto 1:1 line/space patterns. Some of the defects are embedded in array type structures, whereas other are located at the line tip to simulate line extensions, for example. The figure also shows SEM images of the minimum defect size detected with D2BRD inspection in the 20 nm half pitch horizontal patterns (1x wafer). As a reference, the same wafer was inspected using a D2D "Random" defect inspection. The alternating defect and reference blocks present on the mask allows us to define a wafer map compatible with D2D image subtraction of the two types of blocks. All other recipe parameters, including spectral mode, apertures, polarization, and sensitivity thresholds were identical for the two types of inspection for comparison purposes. For ~ 87 % of the 30 different defect types present, D2BRD detection sensitivity was equal or superior to D2D inspection. The corresponding SEM image of the minimum size detected by D2D inspection is included in the Figure for the structure types depicted. The increased sensitivity of the D2BRD methodology is presumably due to the enhanced signal-to-noise ratio that the averaging algorithm affords to the technique.

In Figure 3A, D2BRD detection maps for each of the 30 defect structures present in the mask are plotted as a function of defect size, along with the number of fields it was detected on for the 18 nm half pitch vertical line/space. As a benchmark, the corresponding sensitivity limit for each of the defects using eBeam Die-to-Database inspection with a 5 nm pixel size is depicted in the same plot in red. For ~ 37% of the defect types D2BRD demonstrates superior detection sensitivity than eBeam inspection, and for another 23% it is comparable. Interestingly, D2BRD seems to perform better than eBeam in some of the logic-type defects on the right-hand side of the plot, despite the false detection with low field count that generates some noise in the graph for smaller defect sizes. Verification of actual detection was confirmed by analysis of the patch images from the inspector tool to avoid reporting false detection events. D2BRD inspection also showed higher detection sensitivity than eBeam for opaque defects, which are more representative of mask adder defects (greater sensitivity in 57% of the defects).

Additional insight into the detection capabilities of the D2BRD methodology can be gained by examining the print sizes of the defects by SEM reviewing known defect locations. Figure 3B shows the measured print size (1x) of two types of defects embedded in 18 nm half pitch patterns (1x wafer dimension) with vertical orientation, as a function of the measured mask (4x) defect size. Measurement were taken along one dimension only, as shown in the defect diagram, and are limited by the uncertainty of visual placement of the feature edges. The D2BRD detection sensitivity is included in the Figure, as a reference. The measurements suggest the minimum printed defect size is ~ 35 nm (1x wafer dimension) for both clear and opaque defects presented in the plot, beyond which we only

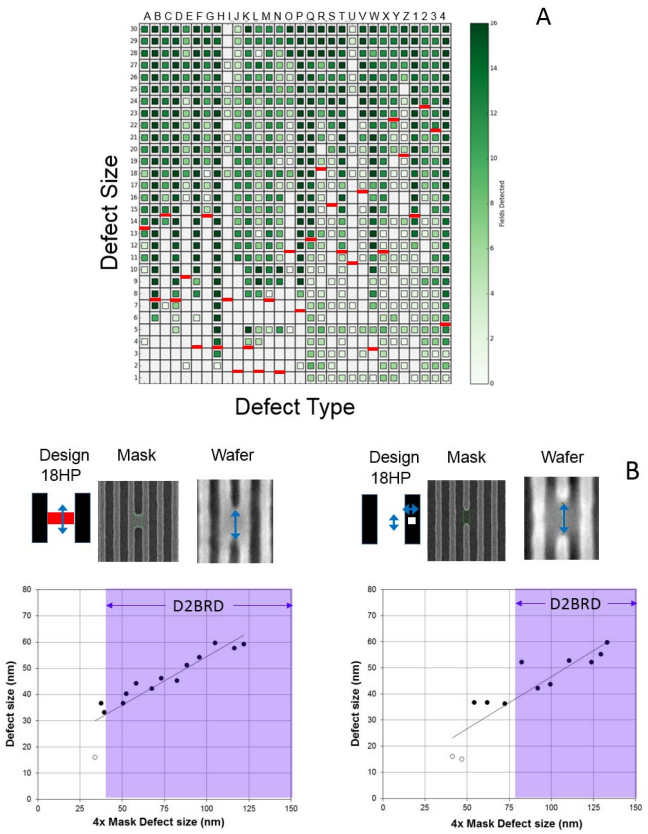


Fig. 3A) Detection sensitivity of D2BRD inspection for 18 nm HP vertical line/space pattern (1x wafer) evaluating 30 different defect types as a function of size. The lines in red depict the sensitivity limit found during e-Beam inspeciton. B) SEM measured (1x) print defect size plotted as a function of the SEM measure (4x) mask defect size for a clear and an opaque defect within 18 nm HP vertical patterns (1x). Empty data points depict impact on line/space width only.

observe an impact on the fidelity of the pattern print, such as line pinching for the clear type defect. The wafer printability threshold might be expected to be lower at the dose used to print an 18 nm (1x wafer dimension) half pitch features on target. Lithographic defect simulations have shown that the printability threshold observed for these and other defects are consistent with the measured mask defect size, as discussed in detail in our earlier publication [3].

Most importantly, we observed that for a wide variety of defects measured, the D2BRD methodology is detecting at or close to the limit of the wafer defect printability threshold, and in some cases, detecting impact on neighboring lines. For the particular cases shown in Figure 3b, the D2BRD detection sensitivity of the opaque 'Pin dot-type' defect than the clear one.

## IV. Full Die D2BRD Inspection: Test Mask

Once the detection sensitivity of the D2BRD methodology was demonstrated, its applicability for rapid and reliable wafer-based mask adder defect detection in the full chip was tested. The test mask used contained 1:1 line/space horizontal and vertical patterned arrays at a variety of pitches, and was cleaned prior to initial EUV exposure of the wafers to remove any potential backside or frontside particle adders [4]. Recipe creation, including the recording of the golden 'reference' image, was performed on a wafer exposed after the mask was cleaned to ensure no mask adder defects were stored in the reference. Thus, D2BRD inspection of wafers exposed in the same lot for repeatability purposes, would be expected to yield no repeater defects. Additionally random D2D inspection of the same wafers was simultaneously performed to gauge the ability of D2BRD to suppress process defects. As a reference, the scan time for the D2BRD inspection is ~ 75 min for complete chip coverage with high sensitivity settings in the inspection recipe (small pixel size, low scan speed, and polarizations). While this is longer than most BBP defect inspections which scan a limited area, it is representative of typical metrology performed before clearing a lot through a section, and significantly less than full die scanning via eBeam inspection (~10 days for 10 nm pixel size). It is important to note that for this mask the D2BRD methodology allowed us to use more aggressive sensitivity settings than our D2D inspection with low nuisance rates due to both the averaging algorithm, and the repeater analysis performed post processing that can be used to filter out undesired detection events, as will be discussed in the following paragraphs.

Figure 4A shows the defect maps resulting from D2BRD and D2D inspection of a wafer exposed with a 'clean' mask. The wafer map for the D2BRD inspection shows a single row, since the averaging algorithm makes defect location for all other dies in the same row identical. Significant process defect suppression is clear when comparing the two wafer maps. Analysis of the defects from both inspections suggest D2BRD can typically achieve process defect suppression rates of around 95 – 98 %. The remaining random process defects can be identified as such by patch image analysis and SEM review, as exemplified in Figure 4b. The patch images for the test die shows the presence of a defect not seen in the virtual reference image, while the SEM image shows no visible defect. Most importantly, the random nature of the process defects makes them inherently non-repeaters, as seen in the histogram plotting the normalized process defect count by the number *R* of defect events at a given location. Thus, these defects can be effectively filtered out by performing a repeater analysis, in which a repeater is defined as any two or more defects found at a given die row location within a 1 um capture cross-section or tolerance.

After removing process defects, there is still a significant number of defects detected in the D2BRD inspection, as shown in the die stack of Figure 4a. This is an unexpected result considering no mask adder repeaters should be found in wafers exposed with a clean mask. Repeater analysis shows most of these defects are present in all 7 die rows (R=7), and SEM review demonstrates the defects are real and are similar to the programmed defects discussed earlier (Figure 4B). Patch image analysis shows that a defect in an otherwise unresolved pattern is present in both test and virtual images, with a variation in pixel count or intensity between the two allowing defect detection. In fact, the defect cluster that appears in the lower right hand corner of the die was previously identified during mask inspection as "native" (inherent) mask defects.

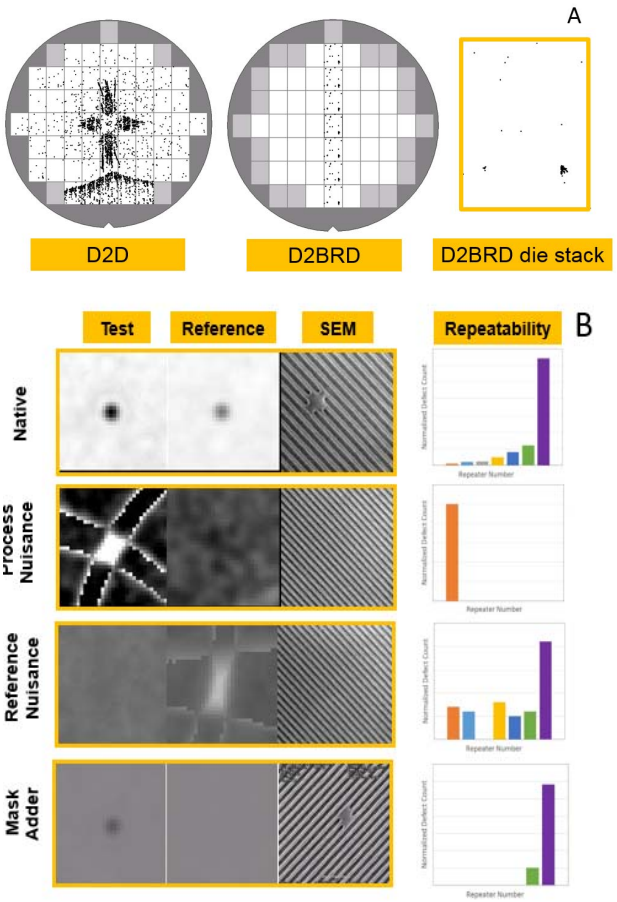


Fig. 4. A) Wafer maps of D2D and D2BRD full chip inspection with a clean test mask illustrating the suppression of process defects. Also shown is the D2BRD die stack after repeater analysis to remove process defects B) Characterization scheme for identifying native mask defects, mask adders, process and reference nuisance based on SEM and patch image review and repeater analysis.

This is one of our earlier EUV test mask that contains an anomalously large number of native defects, uncharacteristic of our current EUV mask standards. However, this anomaly served to prove that the D2BRD methodology can also achieve native mask defect detection when inspecting at aggressive sensitivity conditions, contrary to our expectations. Lithographic simulations presented elsewhere [3] suggest the variable pixel count that allows native defect detection may be a result of a strong focus sensitivity for the defect printing process window.

It is important to note that a small subset of defects detected by the DB2RD methodology are neither process defects from the test wafer, nor native mask defects. These defects are repeaters, but SEM review confirms no defects are found in their location (Figure 4B). Patch image analysis demonstrates the presence of a defect in the virtual reference image only, and not in the test image. This suggests they are process defects that were not suppressed by the averaging algorithm during golden reference image collection.
Once a native defect baseline was established for the test mask, regular monitoring of mask adder defects over the full die area was implemented. A plot of the defect count over several mask cycles shows the first appearance of a mask adder in our 7th regular inspection cycle (Figure 5A).

Mask adders are characterized by being high repeaters and demonstrating a clear defect in the patch image of the test wafer only, and not the virtual reference image, as exemplified in Figure 4B.
The adder defects, which correspond to a single defect on the mask, are of course confirmed to be real during SEM review of the wafer. Further confirmation can be obtained by SEM review of the defect in the mask itself, as shown in Figure 5B. As part of our mask monitoring strategy, Energy Dispersive Spectroscopy (EDS) is also performed to obtain the chemical signature of the defect, to ascertain its origin.

Continuous tracking reveals two more excursions in which several additional particles were deposited on the mask during non-standard mask operations. This is followed by a mask clean, that removes many of the adder defects, and is successfully tracked by our optical D2BRD inspection in the 17th inspection performed.
The regular tracking of this test mask via D2BRD inspection has proven to be an invaluable tool to monitor excursions in the EUV scanner with reasonable inspection times. The methodology can also useful to test and validate protocols for mask handling, cleaning and storage.

## V. Full Die D2BRD Inspection: 7nm Product Mask

The test mask case discussed in the previous section illustrates the potential for using the D2BRD inspection methodology to monitor EUV ancillary processes, such as mask handling and storage. Ultimately, a strategy to enable EUV lithography while ensuring zero

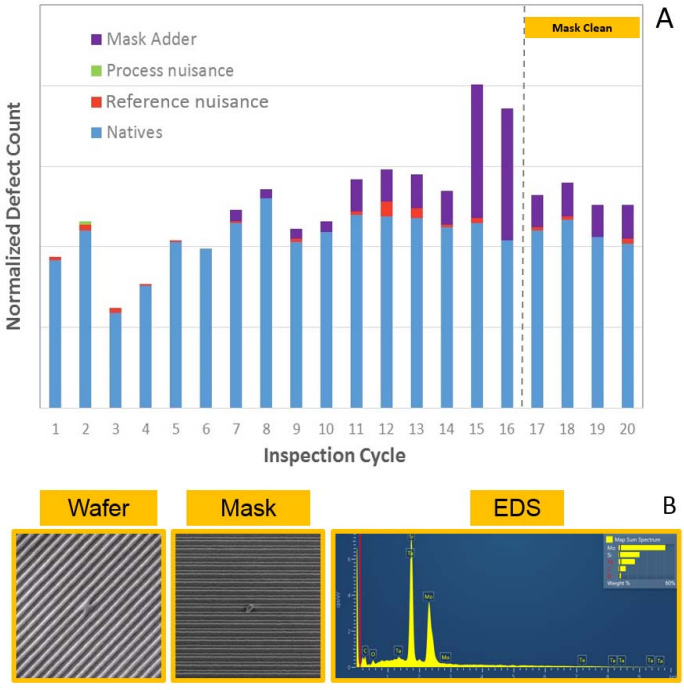


Fig. 5. A) Periodic monitoring of mask adder defects in test mask using D2BRD inspection depicting the successful identification of mask adder excursions events and subsequent mask cleans. B) Wafer and mask SEM images of one of the mask adder defects detected via D2BRD inspection, and its corresponding EDS chemical signature.

mask adders would require the implementation of optical D2BRD for every EUV mask in production on a periodic inspection basis. In this section, we discuss the additional challenges involved in the full die inspection of a Metal 1 level EUV product mask, and the results from recent monitoring activities. In particular, we focus on the difficulties of achieving full die inspection at high sensitivities and low nuisance rates in product masks with a wide diversity of patterned structures. This can only be achieved with high granularity of inspection care areas groups to maximize the coverage the variation of line/space widths in the plurality of designs over the entire chip, and thus calls for a shift in the device-centric paradigm of care area generation.

Conventional defect inspection employs two strategies for inspection detection. In the first case, a single "best guess optimization" threshold is utilized for full chip inspection. In this full chip single care area group approach, the sensitivity of the detection is compromised in order to simply achieve a "best-can-do" inspection sensitivity over the entire chip. In this case, no special care area creation is required. In this second case, care areas are crafted for each type of important device design. In this device-centric care area group case, since the each care area group covers a unique design type, the noise threshold can be uniquely optimized for high sensitivity. This case suffers from the following two limitations: a) the surgical approach to care area generation may require time–consuming crafting of the care area groups b) only a finite (ie. <15-20) number of device designs can be uniquely optimized for noise thresholds. Although this approach gives high sensitivity, it is not amenable to full chip implementation with a wide variety of designs per mask level.

The inspection requirements of both full design space coverage over the entire chip and maximum sensitivity necessitates an alternative approach. This approach requires that care areas need to both cover the maximum area of like pattern design sizes and individual care area grouping are deployed for each distinct design line/spacing type independent of the device. Each care area group is defined by a set of rules akin to design rule check. The care area grouping can be individually optimized for highest sensitivity and lowest nuisance rates. Since the care area groups are rules based, a variety of design type may fall in a single grouping. This approach is not found to largely limit sensitivity defined by the noise detection threshold. Requiring a high sensitivity of detection across the entire chip design over a large but operationally feasible number of inspection care area groupings is found to adequately cover the variety of line/spacing designs for each mask design layer.

An example of care area generation approach used in this study in given in Figure 6A for the metal layer. A large number of care area groups shown in different colors, represent the rules based line/space widths implementation. Some of the designs incorporated into different care area groups based on their line/space widths are also included in Figure 6A. During recipe creation care areas were set to different thresholds as much as possible to maximize sensitivity of the overall inspection. Importantly, recipe parameters are initially set with a D2D inspection run, since few defects of interest can be found in a D2BRD inspection to allow recipe optimization.
After initial parameter selection and storage of the virtual reference die image, a D2BRD inspection is performed to confirm the settings are appropriate for low nuisance rate. Thus, D2BRD recipe creation is a process that typically requires more iterations than regular D2D or array-type inspections.

Despite the granularity of the care area groups generated for full die D2BRD inspections, nuisance rates are higher in our product wafer recipes than in the simpler test mask described earlier, as would be expected from the limited number of regions and thresholds that can be independently set for the various design structures, and the die-sized care area with mixed content that encompasses wiring, open area, etc. Nonetheless, most of the nuisance can still be effectively filtered out via repeater analysis. In this case, there are no known printable mask absorber native defects present within the scanned area. However, using this methodology we have been able to detect one mask adder event of 55 nm (1x wafer dimension) in width, as depicted in Figure 6B. The Reticle Design File (RDF) clip is included since its critical feedback for risk assessment that will determine how the mask will be dispositioned i.e., if the defect lies within a critical macro that requires it to be cleaned. Regular monitoring of this and other product mask is on-going, and will likely shed more light into the utility and challenges of using D2BRD for adder defect inspection of product masks.

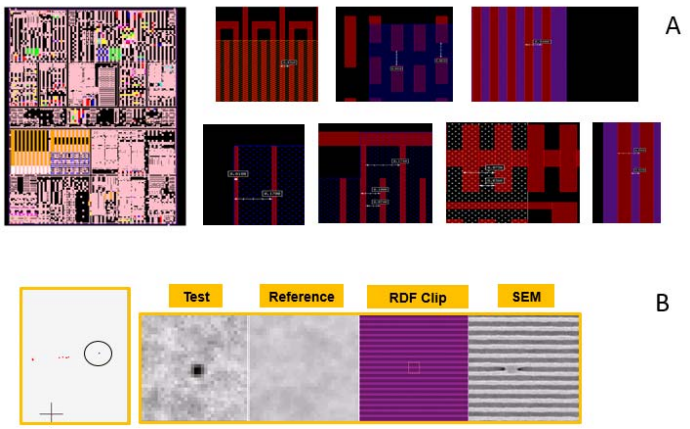

Fig. 6. A) Care areas generated with a DRC-like methodology for the 7nm Metal 1 layer, where each color represents a different care area group. Also shown are different designs incorporated into various care area groups based on their line/space width. B) Mask adder defect detected via D2BRD inspection of the Metal 1 layer

## VI. Conclusions

Building on prior work, we have evaluated an optical inspection technique termed D2BRD designed to detect repeater defects, and have shown impressive detection sensitivities that can rival the detection capability of eBeam inspection for a variety of opaque and clear absorber mask defects, in a considerably shorter scan time. More importantly, we have demonstrated that this wafer-based mask inspection technique can be used to safe guard EUV masks against defect adder exposure. Thus, a comprehensive strategy to enable EUV lithography would begin with qualification of an EUV mask through backside and frontside inspection of the mask (blank and patterned mask inspection), and validation of printability of mask defects on wafer through eBeam inspection. D2BRD inspection can then be used to both corroborate the printability of native defects and, to enable regular monitoring of mask adder defects. The D2BRD methodology that allows full die inspection of both test and product masks can be summarized in the following steps (Figure 7): 1) full die, DRC-like care area generation (in red), 2) an iterative recipe creation process that includes collection of a virtual reference die image (yellow), 3) adder repeater inspection with a test wafer which involves repeater analysis, subtraction of native and mask adders

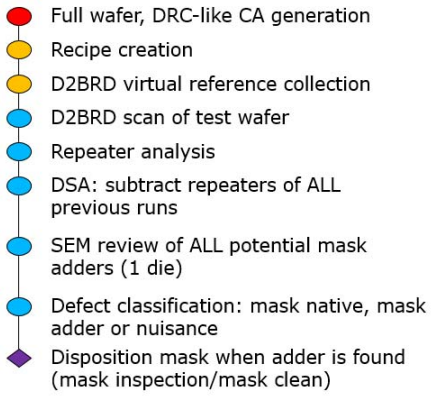


Fig. 7. Schematic representation of the D2BRD inspection methodology.

detected in previous cycles, SEM review of all potential mask adders and classification into process nuisance, native or mask adders defects (blue), and 4) disposition of the EUV mask if an adder is detected (purple).

Future work to verify the robustness of our methodology for mask adder detection in various EUV product masks as a function of use cycles is underway.

## VII. Acknowledgements

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## VIII. References

[1] R. K. Bonam, H. Y. Tien, C. Park, S.D. Halle, F. Wang, D. Corliss, W. Fang, J. Jau. (2014). E-beam inspection of EUV mask defects: To etch or not to etch? *in Extreme Ultraviolet (EUV) Lithography V, Proc. SPIE Vol. 9048* (p. 904812). O. R. Wood II; E. M. Panning, Editors.

[2] R. Bonam, S Halle, D. Corliss. H-Y Tien, F. Wang, W. Fang. J. Jau. (2013). E-beam inspection of EUV programmed defect wafers for printability analysis," In Advanced Semiconductor Manufacturing Conference. *24th Annual SEMI,* (pp. 310-314). IEEE.

[3] S. D. Halle, L. Meli, R. Delancey, K. Vemareddy, G. Crispo, R. Bonam, M. Burkhardt. (2015). Toward defect guard-banding of EUV exposures by full chip optical wafer inspection of EUV mask defect adders. *Extreme Ultraviolet (EUV) Lithography VI, Proc. SPIE, Vol 9422*, (p. 94221D).

[4] L. L. Cheong, L. M. Kindt, C. Turley, D. Leonard, J. M. Boyle, C. F. Robinson, J. Rankin, D. Corliss. (2015). EUV mask cleans comparison of frontside and dual-sided concurrent cleaning. *Extreme Ultraviolet (EUV) Lithography VI, Proc. SPIE, Vol. 9422*. O. R. Wood II; E. M. Panni.