New Ideas for New Materials

**Introduction**

IC manufacturers worldwide are currently producing devices at the 130-nm node with 90-nm-generation products in pilot production, and 65-nm and 45-nm processes under development. Several process and integration issues identified at the 130-nm node have been resolved. However, the 90-nm generation has several unique problems remaining to be solved. Some of the issues that still need resolution include high leakage currents of gate dielectrics, electromigration (EM) and stress migration control in copper (Cu) interconnects, Cu barrier integrity, and Cu electroplating and chemical-mechanical planarization (CMP).

New materials and processing technologies are continuously being evaluated and introduced to resolve these issues. These include metal compounds and alloys, multilayer films and ultrathin atomic layer deposition (ALD) films (Figure 1). The introduction of these new materials has given rise to new process control parameters. In addition to measuring film thickness, controlling the composition (stoichiometry) of these materials is necessary to achieve desired properties.

![Figure 1](image.png)

*Figure 1. A key trend emerging in the semiconductor industry is the proliferation of new CMOS materials. At the 130-nm node, one could find approximately 20 possible materials in use. By the 65-nm node, the list of materials is expected to grow to 34 or more, with such new additions as silicon-on-insulator (SOI) and silicon germanium (SiGe) substrates, ultralow-k dielectrics, hafnium oxide (HfO₂) and silicon oxynitride (SiON) gates, and atomic layer deposition (ALD) barrier and seed layers.*

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Cu Barrier

Cu barrier layers form an important part of the Cu interconnect by ensuring that Cu does not diffuse into the dielectric and cause line-to-line leakage or early time dependent dielectric breakdown (TDDB) failures, and create dark-level defects in the silicon substrate. The effective line resistance of Cu interconnect increases with the thickness of the barrier layer. In order to maintain effective conductor resistivity below 2.2 μm·cm at the 90-nm and 65-nm technology nodes, barriers need to be ultra-thin, so that they consume less than 15 percent of the trench cross-section. Barrier thickness needs to scale from 16 nm at the 130-nm node all the way down to 70 nm for the 65-nm node (ITRS Roadmap 2002).

Physical vapor deposition (PVD) continues to be a viable technology for barrier deposition at the 90-nm node and can be extended to 65 nm as well. However, PVD will not be adequate for the growth of pinhole-free conformal barriers on porous via and sidewall trenches, which requires better control over the barrier deposition process. Barriers for technology nodes at and beyond 65 nm are currently being explored, with the most promising candidates being tantalum (Ta)-based ALD barriers, TiSiN metal organic chemical vapor deposition (MOCVD) barriers and tungsten nitride (WNx)-based chemical vapor deposition (CVD)/ALD barriers. MOCVD TiN has been reported to offer better long-term reliability than Ta; however, it exhibits poor adhesion to low-k dielectrics and poor Cu wetting. The search for new barrier materials is also driven by the interfacial behavior between the barrier and porous low-k materials that may be introduced at the 45-nm node.
Copper damascene interconnect reliability

As Cu interconnects mature, various reliability issues and failure mechanisms of Cu interconnect are being discovered and understood. The most significant reliability issues for Cu metallization are stress migration and EM.

Stress migration

Stress migration in Cu interconnect structures (Graphic 1) is primarily caused by two conditions:

a. Vacancies at Cu grain boundaries and micro voids are created during electroplating due to discontinuous barrier and Cu seed layer.

b. Post-deposition anneals and high chip operating temperatures create conditions for these vacancies to move from low stress areas to higher stress areas to equilibrate stress gradients and cause larger voids at areas with stress concentration.

These problems are further exacerbated by large differences in the coefficient of thermal expansion (CTE) of Cu, barrier, and dielectric materials. Void formation at the via bottom has been reported as the most frequent failure mode due to extensive tensile stresses generated at the bottom via corner due to thermal cycling.

Electromigration

It has been reported that EM lifetimes drop as linewidths narrow and barriers become thinner. EM failures occur as a result of Cu diffusing rapidly at the Cu/barrier interface and between the Cu/silicon nitride (SiN) cap interface due to the “electron wind force” created by high current density in Cu interconnect lines. Cu/barrier interface boundaries have limited adhesion because they lack real metallurgical or chemical bonding. Bi-layer barriers such as tantalum/tantalum nitride (Ta/TaN) may be required to provide good interface bonding in order to improve EM lifetime (see Figure 3, page 4). Additionally, barrier composition (percentage nitrogen in TaN) can affect interfacial diffusion rates of Cu, adversely impacting EM lifetime. Thinning the barrier at the base of the via moves the EM failure mode from the via to the line, where the lifetimes are much longer. The composition of thinner barriers has a more significant effect on diffusion properties, interfacial adhesion and film stress—all of which affect EM (Graphic 2). Barrier composition is currently measured during development using analytical techniques such as Auger spectroscopy and Rutherford Back Scattering. Once a process is optimized and transferred to volume production, composition is rarely, or never, checked unless there is an issue.
**Cu barrier metallurgical challenges**

The Cu interconnect barrier should ideally bond firmly to both the Cu and oxide, while offering adequate diffusion resistance to the Cu. Barrier breakdown causes a sharp increase in line-to-line leakage currents due to Cu diffusion, with the added problem of time-dependent-dielectric breakdown (TDDB). There is usually a trade-off between barrier integrity and its adhesion properties (Graphic 3). Ta has a hetero-epitaxial relationship with Cu and forms a thin amorphous layer at the Cu/Ta interface. This results in better adhesion and seed layer properties. It suppresses stress-induced voiding by reducing the number of interface defects that can act as void nucleation sites. TaN, on the other hand, has demonstrated excellent adhesion to silicon oxide (SiO$_2$)-based inter-layer dielectrics (ILDs). Being an amorphous film, TaN also suppresses Cu migration along the grain boundaries, a leading cause of interconnect failure. Another consideration for a good barrier is its electrical resistivity. Ta, in its β phase, has a resistivity of 150-200 µohm-cm, while thin film PVD TaN has a higher resistivity of 200-250 µohm-cm. CVD or ALD TaN can have much higher resistivity (500–1000 µohm-cm) due to the presence of impurities such as C. The combined benefits of Ta and TaN to maximize adhesion and diffusion resistance with lower in-plane resistivity has led to the consideration of the Ta/TaN bilayer barrier for high yielding, reliable, EM-resistant Cu interconnects.

Barrier composition has emerged as an important parameter that must be monitored during production. As the barriers become thinner, their composition plays a larger role in their functionality (Figure 3). Changes in composition can affect diffusion properties, interfacial adhesion and film stress—all of which affect stress migration and EM resistance along with TDDB in Cu interconnects.

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*Graphic 3. Barrier and cap layer failures due to uncontrolled changes in composition result in electromigration-induced reliability failures.*
Incorrect barrier composition can also result in high via resistance due to changes in the resistivity and contact resistance of the barrier, thus degrading parametric yield.

Conventional metrology techniques do not offer a way to measure composition, and, as a result, IC manufacturers are literally flying blind in production, with respect to controlling the composition of Cu barrier layers. Techniques such as four-point probe sheet resistance or photo-acoustic metrology no longer work effectively because they are unable to separate the individual layers of the bi-layer barrier. Nor can they measure under Cu seed layers on product wafers. Promising new techniques, such as X-ray reflectivity (XRR), require very complex modeling algorithms and curve fitting. XRR also lacks the small spot size required for product-wafer monitoring.

Identifying a method that is capable of monitoring Cu barrier composition inline is therefore essential, as it offers an early warning system for potentially expensive IC reliability failures in the field.

**Ultrathin ALD barriers**

To move beyond the 65-nm technology node, ultrathin barriers are required to minimize the barrier’s impact on line-to-line and via resistivity. It is believed that barriers can be thinned to as low as 10-20Å and still provide adequate protection against Cu diffusion into the dielectric region. Significant improvement in line resistance has been observed using PVD and CVD techniques, when the via bottom coverage was minimized. To achieve this improvement with conformal sidewall coverage, IC manufacturers are beginning to explore ALD technology for barrier deposition for the 65-nm and 45-nm nodes (Figure 4). ALD has the capability of providing conductive films at low temperature, with excellent step coverage, low defect density and contamination, and good thickness uniformity and thickness control. Ultra-thin ALD barriers can provide 100 percent step coverage with less than 15Å thickness and less than 3 percent, 1-sigma non-uniformity. Evaluation of diffusion properties has shown that even 10Å of ALD TaN is a better diffusion barrier than 50Å of PVD TaN barrier. Hence, an ALD TaN barrier can reduce via resistance by up to 40 percent and line resistance by up to 25 percent, resulting in a significant reduction in RC delay. Other applications of ALD include the tungsten (W) nucleation layer and electrode films in memory structures.

**ALD process control challenges**

Ultra-thin barriers are deposited in ALD reactors by alternately flowing reactant gases in short duration pulses that lead to the monolayer adsorption of reactant species followed by reaction on the substrate surface to form the desired film. The complexity of controlling the ALD process is similar to that of a CVD reactor as outlined in the previous section. In addition, gas pulse conditions and pulse time cycles in ALD reactors have to be controlled very accurately to ensure optimal monolayer formation and reaction. Also, the ALD process suffers from a variable incubation time in the reactor that can lead to fluctuations in film thickness in production. Surface cleanliness can change the chemistry at the interface leading to excursions in composition. Due to their atomic scale thicknesses, ALD films are more sensitive to changes in thickness and composition compared to thicker films produced by PVD and CVD techniques. Changes in film properties can seriously impact device performance and must be carefully monitored in production. Ultimately, good barrier performance at every location in the device can only be guaranteed through thickness and compositional uniformity inside the trench structures across the wafer.

Currently, the ALD process does not have a good metrology technique available for process control. Conventional four-point sheet resistance measurement punctures through the ultra-thin ALD films and cannot be used for monitoring an ALD process. X-ray reflectivity can be used to determine film thickness, but has poor signal-to-noise for high throughput measurements and suffers from a large spot size for production monitoring. Optical techniques suffer from the problem of correlated...
changes in thickness and optical properties for ultra-thin films and cannot be used to measure a barrier/seed layer film stack on product wafers under an opaque Cu seed layer. Opto-acoustic techniques rely on propagation of a sonic pulse through the film reflecting off the interface, and the transit time in an ultra-thin film is too small to be detected reliably by available instruments.

Electroplating

Electroplating is currently the process of choice for filling vias and trenches for copper interconnect fabrication. It will continue to be used for the 90 nm and 65-nm nodes due to its ability to uniformly and adequately fill narrow and high aspect ratio trenches without pinch-off at the top of the trench.

Electroplating process control challenges

The electroplating process typically uses an accelerator and suppressor in the form of a short or long-chain polymer to provide bottom-up fill in small vias and trenches. Surface topography control during the electroplating process is a key issue, since the additives required to ensure filling often result in so-called “super-filling,” where the thickness of the overburden of Cu is higher on densely patterned areas (Figure 5). Super-filling leads to residual metal in the field areas due to non-uniform removal during Cu CMP, especially in dense patterned areas.

Another important parameter, global plating thickness uniformity, depends on being able to deliver adequate current uniformly across the wafer during plating, especially to the center of the wafer. This is a more significant issue for larger wafers and thinner seed layers due to the higher resistance that results in a drop in the plating over-potential at the wafer surface, affecting local deposition rates. Employing higher plating currents could result in thicker Cu deposition at the electrode contact points, leading to residual metal or flaking during the CMP step.

Thickness and uniformity measurements of Cu after plating are currently carried out using either a contact sheet resistance method or non-contact methods such as opto-acoustic or X-ray fluorescence. A non-contact method of measuring Cu thickness also needs to have high spatial resolution to be able to measure die-level microvariations of thickness due to super-filling and more global variations across the wafer and very close to the edge of the wafer. A large variation in the plating current at the edge can cause a thick “edge bead” of Cu, which can create difficulty during CMP removal by leading to over-polishing in the center of the wafer.

Voiding of vias and trenches continues to remain an issue for electroplating due to aging of the electroplating bath and changes in the concentration of additives caused by the degradation effects of time and temperature on the organic long-chain polymers. As feature sizes continue to shrink, voids in the vias and trenches can migrate to the interfaces and increase the chances of EM and stress migration failures in the Cu interconnect. Therefore, it is crucial to detect sub-surface partial voids to offer an early warning system for reliability failures. Random voiding of trenches and vias, especially in known problematic structures, can be monitored in production using electron-beam inspection of a via chain array in a test structure.

Alloying elements such as tin (Sn) are being tried out at the 65-nm node to improve the EM resistance of Cu interconnects, although it comes at the cost of increased
line resistance. Composition measurement and control of the Cu alloy will become critical to achieve the desired EM resistance while maintaining the resistance of the Cu lines.

**Cu CMP**

Chemical mechanical planarization (CMP) of Cu is the only viable approach for removing copper and barrier from the field areas after plating to leave copper-filled trenches forming the interconnect. Although Cu CMP was introduced at the 0.18 µm-node, it remains a relatively immature, highly empirical process, dependent on quality and stability of the consumables used in the process. Cu CMP process control issues and challenges are exacerbated at 90 nm and below due to increasing metal line density and shrinking dimensions of the interconnect.

**Cu CMP process control challenges**

While there are several issues associated with Cu CMP, process control is mainly focused on reducing topography caused by dishing of large features, dielectric erosion in dense arrays, excessive metal loss due to over-polishing, or residual metal due to under-polishing (Figure 6).

Dishing and erosion result in copper loss in the lines and, hence, an increase in the sheet resistance. Additionally, topography generated at the lower metal layers carries over to the upper levels and creates copper pooling that does not clear even after long overpolish. This issue is more challenging as the number of metal levels continues to increase to as many as 10 for advanced technology nodes. Beyond 90 nm and 65 nm, post-CMP topography could also impact depth of focus during the dielectric lithography step. For the 65-nm node, the ITRS Roadmap 2002 (page 75) requires erosion of a 50 percent metal density array to be less than 13 nm, and dishing of 100 µm lines to be less than 19 nm in order to maintain the required sheet resistance of the Cu interconnects.

Cu CMP involves the use of several consumables, such as slurries, pads, pad conditioners, corrosion inhibitors and cleaning chemistries that add variables to the process. Changes in slurry composition, agglomeration or settling of abrasives and variations in oxidizer dosing can cause significant drift in dishing, erosion and uniformity. Drift in uniformity leads to longer polish times that, in turn, can degrade topography. The age of the polishing pad and inadequate pad conditioning can result in underpolishing, leading to residual metal. Therefore, process qualifications, including topography and defectivity verification, have to be made after every consumable change.

For these reasons, CMP is probably the fab’s most metrology-intensive process, with metrology time accounting for almost 50 percent of tool downtime. Sheet resistance measurements are currently used on blanket wafers to determine polish rates and selectivities. However, in order to maintain tight control of the process, ideally both post-CMP topography and Cu thickness measurements on product wafers are essential. While profilometry can be used to measure topography, it cannot measure the thickness of Cu remaining in the trenches. Topography measurements will have to be combined with oxide thickness measurements in arrays to derive the thickness of the neighboring Cu lines. Resistance measurements can be used to derive the thickness of Cu lines; however, they do not provide information on dishing and erosion-related topography. Opto-acoustic techniques are being actively investigated for Cu CMP measurements. While they can be used for a wide range of film thicknesses (40Å to 3 µm), they may experience interference from the underlying films and, hence, have limitations in measuring multiple metal levels.

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**Figure 6.** Cu CMP process control is mainly focused on reducing topography caused by dishing of large features and dielectric erosion in dense arrays.
Electroless capping layer deposition

Copper interconnects at the 130-nm and 90-nm nodes are surrounded on three sides by a diffusion barrier and capped on top by a silicon carbide (SiC) or SiN layer that acts as a passivation and barrier layer to prevent copper oxidation, corrosion and diffusion, as well as an etch stop layer in Cu/low-k integration schemes. As the dimensions of the interconnect are scaled down, the ratio of Cu surface area to volume increases. This makes interconnects more susceptible to surface diffusion-related EM phenomena that cause leakage and EM failures.

New capping materials (Figure 7) are being investigated to reduce the interface diffusion of Cu, and the most promising candidate so far is cobalt tungsten phosphide (CoWP). Improved EM behavior of up to a 10-fold increase in lifetime has been demonstrated using a 10-nm electroless CoWP capping layer to achieve a significant reduction in Cu interface diffusion.

EM failures in the form of line-opening voids can happen in two modes: line depletion, where the void forms in the middle of an interconnect line, and via depletion, where the void occurs at the via interface with the underlying or overlying interconnect. Cu lines can often fail due to line depletion EM mode and a weak interface between the Cu line and the dielectric at some point along the long interface. With the addition of the CoWP cap layer, the failure mode shifts from line depletion to via depletion mode, eliminating the Cu/cap interface as the weakest point of interconnects.

Electroless cap layer process control challenges

Thickness and composition of the cap layer impacts Cu diffusivity, interfacial adhesion and film stress of the layer and, thereby, its effectiveness as a capping layer. These parameters must be optimized during development and continue to be monitored during production. Pattern dependent loading effects during capping layer growth using a selective electroless deposition process can result in variations in thickness and composition on lines with different feature sizes. The metrology tool used to monitor the film must be flexible enough to measure narrow and wide lines with equal precision and accuracy.

Conventional techniques, such as opto-acoustic and X-ray reflectivity, have a difficult time measuring thin
High-k materials and process control challenges

For high performance applications at the 65-nm node and below, new materials with higher dielectric constants (Graphic 4) will be needed to reduce the leakage currents to less than $10^{-7}$ A/cm$^2$ for the same equivalent oxide thickness (EOT) of ~1.0 to 1.5 nm while maintaining the same gate capacitance and with no degradation of carrier mobility (ITRS Roadmap 2002, page 56). Cylindrical, stack and deep trench capacitors DRAM capacitors are being extended to less than 100 nm using new high-k dielectric materials to reduce cost and yield issues (Graphic 5). Advanced logic gates for low power transistors are also being fabricated with materials that have several orders of magnitude less leakage than SiON. Some of the high-k materials being considered for these applications are ALD Al$_2$O$_3$ and laminates of Al$_2$O$_3$ and HfO$_2$ to further increase the $k$-value for 65 nm and beyond$^{11}$. Other promising materials under consideration are HfAlON and HfSiON. Al, Si, and N elements help to stabilize the structure, control boron diffusion and improve carrier mobility. Hence the concentration of these elements and the film thickness must be measured and controlled to provide consistent gate performance.

Such hybrid and compound materials necessitate the use of ALD technology for controlled thin-film deposition. A benefit of ALD is that it provides the ability to engineer the composition throughout the thickness of the film to provide the right properties at each interface. In addition to thickness and composition control to achieve EOT scaling, composition control is also critical to tune band-gap and mobility which remains a major challenge. Gate composition also affects thermal stability and boron penetration through the gate and other integration issues.

Along with the benefits come several processing and process control challenges, such as finding the right precursor and controlling the impurities in the film. Since ALD is a slow, low temperature process, it is easier to introduce impurities that can significantly change the composition and properties of the film, considering that the films themselves are only a few atomic layers thick. The only techniques currently used to monitor thickness and composition of ALD films are X-ray reflectivity and X-ray fluorescence, both of which are not available for inline measurements with the spot-size, throughput and precision required for production monitoring.
CoWP layers on Cu interconnects due to the low density contrast between the Co alloy and the underlying Cu, which provides a weak return pulse to the surface or does not reflect enough X-rays at this interface, resulting in a poor detected signal. Furthermore, these techniques cannot measure the composition of the CoWP layer, which has an important effect on its EM-enhancing capability.

**FEOL considerations — new gate materials**

As feature sizes shrink and gate oxides get thinner, gate leakage current increases exponentially. Currently, lightly-doped silicon oxynitride (SiON) is being used in production at the 130-nm node. SiON with higher amounts of nitrogen (N) incorporated through plasma nitridation is the choice of gate dielectric material for the 90-nm node (Figure 8). The amount and distribution of N that is incorporated into the gate oxide is a key factor in controlling electrical performance. Some of the process parameters that could cause a drift in the N concentration include RF power, gas pressure, and flow ratio of the plasma nitridation reactor.

**Process control challenges of monitoring N distribution**

Although optical techniques offer a fast non-contact method of monitoring thickness and N dose on product wafers, they do not independently resolve changes in thickness and N concentration. Required is an independent method of monitoring N dose and thickness for process development and excursion recovery in production. X-ray photoelectron spectroscopy (XPS) can be applied to measure N dose in ultrathin SiON gate dielectrics, but it has been mostly used as an off-line analytical reference technique due to its requirements of very high levels of vacuum and a large spot size. The surface selectivity of XPS also makes it susceptible to under-estimation of the N dose when the N is piled up at the interface (as in RTNO processes) or an over-estimation of the N dose when it is piled up at the surface, as in high-density plasma nitridation processes.

**A new metrology solution for opaque films**

A new electron stimulated X-ray (ESX) metrology technique now available on KLA-Tencor’s MetriX 100 platform addresses the needs of the 90-nm node and beyond for measuring thickness and composition of a wide variety of films on product wafers.

The tool’s incident electron beam causes characteristic X-rays of the elements present in the measured film stack to be emitted from the material (Figure 9). Film thickness is calculated by measuring the intensity of the elemental X-rays. For a compound film, the composition can be calculated by the ratio of the X-ray intensities of the elements that make up the compound. The electron beam column of the MetriX 100 delivers high beam current (up to 2 mA) with a broad range of landing energies (0.5-30 kV) and a selectable spot size from 10-30 mm, suitable for product wafer metrology. The electron beam has a high beam current to generate sufficient photons for enhanced precision at high throughput, since the measurement precision error is inversely proportional to the square root of the photon count (Poisson statistics). The landing energy is selected based on the materials and film thickness being...
measured and can be tuned for a wide range of elements and film thickness (Figure 10). Typically a landing energy of two-and-a-half to three times that of the highest energy line being measured is selected to maximize the generation of X-rays for high precision. Thicker films may require higher energy, because the electrons lose energy as they travel through the film due to collisions with the atoms of the film.

The X-rays from the different elements in the film stack can be discriminated through an X-ray detector by their characteristic wavelengths or energies. While a single solid-state energy dispersive detector can be used to quickly identify all the elements present in the film, this type of detector has relatively poor spectral resolution and a low signal-to-noise ratio, resulting in spectral interference and poor sensitivity. The MetriX 100 uses multiple wavelength dispersive X-ray detectors, or spectrometers, to measure the X-ray counts emitted by each of the elements in the measured film stack (Figure 11). Each spectrometer is designed to detect a specific wavelength of an elemental X-ray line and quantify it. The MetriX 100 incorporates up to six customized spectrometers, thus allowing a range of elements to be covered by the system.

Wavelength dispersive X-ray detectors, or spectrometers, have a very good signal-to-noise ratio and spectral resolution of the X-ray peaks and are, therefore, excellent quantitative detectors. The superior signal-to-noise ratio provides higher sensitivity to lighter elements such as O and N. High measurement precision and
throughput can be obtained due to the high count rates of the detectors and low detector dead time. As a result, the MetriX 100 provides a thickness measurement repeatability of <1% 1-sigma for ultrathin films down to 20Å thickness and a composition repeatability of <1-2% 1-sigma, even for a light element such as N. These features make the MetriX 100 highly suitable for fast, non-contact measurement for monitoring product wafers.

Case studies

TaN Cu Barrier excursion: An excursion in the via resistance of a TaN/Cu 130-nm Cu barrier seed metal layer was observed at end of line (EOL) electrical probing. The thickness profile of the TaN was measured using a conventional opto-acoustic measurement system, and did not reveal any difference in thickness compared to a known good baseline wafer with normal via resistance distribution. The wafers were then measured using the MetriX 100 system for thickness and composition and compared to the baseline wafer. Figure 12 clearly shows the difference in the composition of the barrier compared to the baseline that is not detectable in the comparison of the thickness profile. The percentage N composition measurement capability of the MetriX 100 system thus proved essential in detecting this excursion in-line. The excursion in percentage N in the TaN barrier was then traced back to the PVD reactor due to an improperly installed process kit that was subsequently rectified.

Gate SiON dielectric plasma nitridation design of experiment

A design of experiment (DOE) on a SiON plasma nitridation reactor was performed to characterize the percentage N incorporated in the gate dielectric. The percentage N in SiON controls the leakage of the film and, therefore, the standby power consumption of the transistor. An excess of N results in a degradation of channel mobility and, hence, transistor speed. The optimum conditions for a plasma nitridation process—RF power, pressure and time—were characterized by the percentage N dose that gives the optimum transistor performance (Figure 13). The N dose was correlated to an existing lab baseline of XPS for a variety of processes (Figure 14). The MetriX 100 system also measured the oxygen content of the gate SiON, which correlated well to the existing baseline of measured optical thickness. This combination of N and O measurements allowed inline monitoring of thickness and leakage of the gate dielectric. Optical measurements are faster and sensitive to monitor excursions; however, they do not provide the capability to independently measure N concentration—which allows the plasma nitridation process to be “re-centered” after an excursion.

Figure 12. Process excursion of Cu barrier layer due to improperly installed process kit resulted in high via resistance.

Figure 13. The optimum conditions for a plasma nitridation process—RF power, pressure, and time—were characterized by the percentage N dose that gives the optimum transistor performance.
**Cu CMP process control**

The MetriX 100 system can be used to measure remaining Cu thickness in interconnect structures after a Cu CMP process. Residual Cu or barrier thickness in the field due to under-polish can also be measured. Over-polish can result in a drastic reduction in interconnect Cu thickness, resulting in a drop in line resistance. In addition to Cu thickness, thickness of the barrier under the Cu can also be measured. Figure 15 shows measurements of remaining Cu using the MetriX 100 that correlate well to a profilometric measurement of dishing. Figure 16 shows measurements of Cu thickness in an array and the barrier thickness under the Cu for M1. Figure 17 shows measurements at Metal 3, which pointed to excessive dishing and non-uniform barrier deposition for a new 90-nm process. The information was then used to optimize the PVD barrier deposition process and the Cu CMP polish uniformity.

**ALD TaN Cu barrier characterization**

The MetriX 100 system was used to study the growth rates and composition of ALD TaN barriers on various substrates. Figure 18 shows the change in composition with thickness. As the ALD TaN film grows thicker, it incorporates more nitrogen. Figure 19 shows the variation in ALD TaN growth rates and composition on different substrates. An ultrathin sub-20Å TaN film on Si has significantly lower N content than the same film grown on a SiO2 underlayer. Using this information, the ALD process with the right thickness and composition was selected for further process integration studies.

**Process control of CoWP electroless passivation layers**

Since MetriX 100 was the only tool that could provide independent thickness and composition measurements on features with different pattern densities, an IC manufacturer used the tool to optimize a CoWP selective electroless deposition process for thickness and composition. Optical, photo-acoustic and other analytical techniques had achieved little success. A CoWP cap layer was deposited using a selective electroless deposition process on a blanket Cu wafer. Figure 20 shows a simultaneous six-parameter measurement...
with the MetriX 100 system with thickness of CoWP, Cu and TaN barrier and CoWP composition reported. The measurements were used to optimize the process, and then repeated on a patterned wafer with several test sites of varying pattern density. Because the selective electroless process is affected by pattern loading, the

Figure 16. Post Cu CMP interconnect Cu and barrier thickness measurements in an array.

Figure 17. Remaining Cu thickness increases and TaN/Ta thickness decreases from wafer center to wafer edge.
thickness and composition of the CoWP layer could potentially change due to pattern density effects. Three sites on each die were measured for thickness and composition of the CoWP film as shown in Figure 21. Further adjustments were made to the process until an acceptable within-wafer variation in composition was achieved. By using the MetriX 100, the fab was able to quickly optimize their process to provide uniform thickness and composition on areas of varying pattern density. These measurements can be made inline on product wafers to identify excursions in composition within wafer and from wafer to wafer for different pattern densities.

**Conclusion**

The introduction of new materials and processing at the 90-nm and 65-nm nodes has given rise to several unique problems. This has resulted in new process control parameters. Of these, controlling the composition of advanced thin films is recognized to be crucial for assuring high yield and...
device reliability. Current metrology technologies lack the full capability to monitor both film thickness and composition in production. A promising new technology in the form of electron stimulated X-ray metrology is now available on KLA-Tencor’s MetriX 100 system. Designed for both process development and fast inline production monitoring, this system helps chipmakers achieve control of advanced materials and associated processes.

References