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The road to success is paved with new solutions.
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New Solutions for New Challenges:

A recent article in the Financial Times on the growth of cellular phone usage in Japan featured a photograph of hundreds of Japanese teenagers flashing their cellular phones to capture an image of their prime minister delivering an impassioned speech. For these young fans, the latest in digital technology offered the chance to hoard their own slice of history, instantly.

Take a look around you, and it quickly becomes evident that digital consumer electronics have become an integral part of our everyday lives. From digital cameras and cellular phones to personal digital assistants (PDAs) and high-definition televisions (HDTVs), digital consumer products are making the world more wireless and connected.

New applications for digital consumer electronics arise nearly every day to address new needs. Whoever would have thought the need or desire to use their cellular phone as a camera to take, transmit and receive pictures, like the Japanese teenagers mentioned above? Yet, markets for such applications are emerging, and with digital consumer electronics becoming increasingly indispensable, you need not stretch your imagination too far to see a future where color displays are embedded in appliances and furniture; where freeways are controlled by vast electronic networks to ensure smooth traffic flow and minimize accidents; where future generations of cars will probably have drive-by-wire systems not unlike Boeing 777s; and, where an entire forensic laboratory can be built onto a microchip. In the more immediate future, Intel envisions a seamless, wireless home network that can handle music, photos, and video content available anytime, anywhere and on any device in the home.

In this increasingly digitized world, having an electronic device that is anything less than 100 percent reliable is not an option. The financial and personal loss caused by the widespread occurrence of devices that are unreliable or fail altogether in the field would be truly grim. However, while the reality of a fully connected world is still years away, the prospects of poor device reliability and product failure in the field are here today. As the semiconductor industry ramps to 90-nm production and engages in process development at the 65-nm node, reliability-related problems such as micro voids, electro-migration, stress migration, de-lamination and cracking, can no longer be contained in development, and are arising at random during production. The introduction of dozens of new and exotic materials at these design rules to augment device performance and speed, such as silicon-on-insulator (SOI), strained silicon, atomic layer deposition (ALD) barriers and new metal compounds, present their own unique process integration issues that ultimately can further impair reliability. And while these issues will not cause flying commuter vehicles to crash into the Earth today, they present very real obstacles to realizing the dream of a truly interconnected world.
Going beyond 90 nm

This latest issue of Yield Management Solutions, explores several radically new process control methodologies that are being implemented to help chipmakers address these reliability issues. Our cover story, Eliminating Buried Yield Killers (page 13), presents a compelling argument for implementing e-beam inspection in development, ramp, and production to mitigate new sources of reliability problems. Taking Control of the Copper Process (page 23) explores new metrology techniques—including inline copper interconnect metrology—to minimize the impact of process variations on long-term device reliability and short-term yields.

So, while the technology visionaries out there are dreaming up a new world order, your fortune cookie indicates that there are new process control solutions you can take advantage of to bring the latest generation gizmos and gadgets to market in time to meet the demands of tech-hungry consumers.

Happy New Year!

Uma Subramaniam
Editor-in-chief
Taking Sides to Optimize Wafer Surface Uniformity

Backside Inspection Applications In Lithography

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As the semiconductor industry ramps to sub-130 nm production capacity, the need for optimal uniformity across the wafer surface becomes a very important topic in lithography. Due to the tightening of depth of focus requirements the process window required to be able to print the required structure leaves little or no room for any localized deviation in the wafer uniformity. For 300 mm semiconductor device manufacturing, this resulted in the use of double-side polished, sometimes called “super flat” wafers.

This paper will discuss methods to identify yield relevant defects on the wafer backside without having to sacrifice wafers. It is based on recent studies carried out at both Infineon Semiconductor 200 and 300 mm fabs in Dresden to characterize the need and the effectiveness of wafer backside defect inspection using the backside inspection module (BSIM) on the Surfscan SP1DD.

Introduction

In contrast to bare wafer inspection strategies, semiconductor manufacturers are still in the early learning stages of implementing backside inspections of silicon wafers. Backside defects in the form of particles or topography are highly relevant to photolithography processing. Particularly in 300 mm photolithography, where double-sided polished wafers are used, such defects reduce surface uniformity and cause undesired effects on the exposure chuck. The two most common effects are focus spots and vacuum failures. For critical lithography layers with small process windows, focus spots have a direct impact on yield. Vacuum failures result in tool downtime, which impairs manufacturing efficiency. Moreover, backside contamination often results in time-consuming cleaning procedures of the exposure tool chuck. Experience indicates that 200 mm and 300 mm manufacturing share largely the same backside issues.

The effects that backside defects can have on the devices built on the frontside of the wafer are largely known, but have not been systematically characterized. This is mainly because traditional backside inspection methods require wafers to be manually turned upside down with a vacuum wand to conduct a thorough inspection, which damages the devices on the frontside and could contaminate the inspection tool.

Working with KLA-Tencor, Infineon Semiconductor investigated the effectiveness of a new inspection methodology for identifying yield-relevant defects on the wafer backside in an automated and non-destructive way at its 200 mm and 300 mm fabs in Dresden.
Methodology

The first step in implementing backside inspection is to analyze the surface quality of the wafer backside and determine the sensitivity required for capturing defects of interest (process tool fingerprints). We did this by depositing polystyrene latex spheres onto the backside of a test wafer and adjusting the recipe parameters to achieve at least a 3:1 signal-to-noise ratio.1

For our first experiment, we investigated the backside quality of 300 mm double-sided polished process wafers before and after lithography. The backsides were inspected using a KLA-Tencor Surfscan SP1 unpatterned inspection system with a new backside inspection module (BSIM) option. BSIM employs edge-only automated wafer handling throughout the measurement process, so it enables product wafers to be flipped and measured without destroying the un-scanned side. Double-sided polished wafers can be treated the same as bare silicon wafers, with the exception that they have a higher defect threshold value. This value is dependent upon the desired resolution for detecting tool fingerprints (Figure 1) and data management limitations. For this study, the optical configuration used on the SP1 included the oblique incidence mode and P-U-U polarizations. Defect thresholds were between 0.5 µm and 1.0 µm.

The goal of our second study was to identify the root cause of systematic focus spots detected on 200 mm patterned wafers at various stages in the front end of the manufacturing process. The frontsides of the product wafers were measured inline on a KLA-Tencor AIT II double darkfield illumination system. Defect review and characterization were carried out on a CRS confocal microscope. Offline data analysis, including correlation between front- and backside defects, was done using Klarity Defect software. The backsides were measured on an SP1<sup>DS</sup> inspection system with BSIM capability. The SP1<sup>DS</sup> has the same functionality as the SP1 for darkfield measurements, but provides increased overall sensitivity. For rough 200 mm wafer backsides, the best results were obtained using S polarization for both the incident light and dual (wide and narrow) collection channels. To further suppress background scatter and enhance the signal-to-noise ratio, a 20 or 40 degree aperture was employed. The defect threshold was set between 0.2 µm and 0.3 µm.

Next, we created a database of tool fingerprints from all of the process tools. This is usually done during tool qualification. Using the BSIM option reduces the number of test wafers needed, since the same wafers can be used for front (PwP) and backside contamination tests.

Results and Discussion

Study 1: Characterization of backside properties on 300 mm wafers

For this study, we created one recipe for pre- and post-lithography inspections maintaining its sensitivity to typical signatures. Three lots were flagged for inspection at critical lithography steps. All wafers were measured before and after lithography on the SP1 BSIM using the same recipe. The lot results were mirrored on the tool and sent to the fab-wide defect database in KLA-Results Format (KLARF).

Data analysis revealed that the number of backside defects added to the wafers between adjacent lithography steps (Figure 2) were considerably higher than the number added during the lithography process (Figure 3). Furthermore, we observed that the backside defect count steadily increased throughout the manufacturing process on all lots.
We also found that defect density was affected by the wafer’s position in the lot. The first wafers tended to have the most backside defects, followed by wafers that were handled more frequently during the process flow. This tendency (Figure 4) was seen on all lots at each inspection point. We interpreted this to be the result of the “cleaning effects” that the first wafers in a lot can exert on production tools.

Overlaying the backside defect maps of all measured wafers (Figure 5, left) showed a considerably higher backside defect count than the stacked defect maps of wafers that were not handled as often (Figure 5, right). This step allowed us to establish the baseline defectivity so that process excursions could subsequently be readily detected.

**Study 2: Finding the source of focus spots**

Systematic focus spots were previously identified through patterned wafer inspection and manual classification. Since the focus spots were visible at multiple layers, the actual source was not immediately obvious. However, backside contamination was considered a possibility, since the defect signature appeared in the same position on each layer. A tool commonality study was first conducted to determine the source, but did not reveal a clear candidate. Finally, a systematic investigation of backside defects (using the SP1 with BSIM) and their correlation to the front side revealed the root cause of the problem.

In this investigation, the wafers with systematic focus spots were measured on the SP1 with BSIM in high sensitivity mode. The defect result files were then “mirrored” using software on the SP1 and transferred to the defect database for analysis. The backside wafer maps all showed distinct wafer handler signatures, which could be compared to the fab’s previously established database of process tool fingerprints (in the form of patterned wafer maps). The patterned wafer maps were then overlaid with the mirrored SP1 wafer maps. Defects common to both maps were flagged for further review to determine their size, height and type (Figure 6). These defects — most of which were several microns in size and depth — were identified as holes caused by damage to the silicon on the backside of the wafers, as shown in Figure 7.

We concluded that this damage was the cause of the focus spots. A comparison of the inspection wafer maps with the process tool fingerprint catalogue identified the wafer handler type responsible for causing the defects. Several handlers of this particular type were later found to be damaging the wafers, which explained why the tool commonality study was not successful. By
studying the defect mechanism, we determined that the defects were also being enlarged through subsequent process steps, thereby increasing their impact on the devices on the frontside of the wafer.

Once the source was identified and the defect mechanism understood, a simple modification to the wafer handler solved the problem. The yield impact of this defect mechanism was determined to be one to two percent for each affected wafer over a ten-week period until the root cause was fixed.

**Going forward**

Preventing backside contamination from creating problems in the first place is ideal. Although backside contamination is present at all layers, it is not always relevant to yield. Adding a clean to remove backside contaminants can become costly, and does not remove all defects. In addition, scratches and pitting can sometimes be made larger by the cleaning process. Thus, it is important to know when corrective action should be taken.

A good place to begin is at the most critical lithography step, or at the step that has the most focus spots. As with traditional pattern wafer monitoring, only a sample of wafers is inspected. A monitoring strategy should also include excursion control and baseline defectivity reduction programs.

**Prevention of focus spots**

**Pre-lithography — Backside Inspection:** The goal here is to determine whether large random backside defects exist on the wafers that could cause a problem during the lithography process, and, if so, trigger corrective action before the wafers reach the exposure tool. A sample of five to ten wafers can be taken per lot depending on defectivity level and variability. Random defectivity should be separated from tool fingerprint signatures, and large particles should be separated from small particles. Thus, a backside clean will only be triggered when large, random defectivity occurs in order to avoid tool aborts and random focus spots. The collected data is sent to the defect database for further analysis, since systematic focus spots cannot be removed by a clean if they are caused by damage (Figure 8).

**Post-lithography — Frontside/Backside Inspection:** Here, the goal is to identify whether focus spots are generated during lithography, and, if so, trigger appropriate corrective action, such as a chuck clean on exposure tools and rework of the affected wafers. Inspection is carried out on macro-defect or micro-defect inspection tools using the same wafers as above to conduct pre- and post-comparisons. Focus spots are separated from other defect types, and will trigger a backside inspection based on the number of identified focus spots. The data is sent to the defect database to be overlaid with the mirrored backside wafer maps from the pre-lithography inspection step (Figure 9).

**Wafer backside signature analysis**

It is clear that the particle or defect signatures on the wafer backside are key to identifying the root causes of
a particular issue. The next logical step is to automate current manual steps. The difficulty in achieving this lies in being able to separate and automatically classify the individual signatures without treating them as clustered defects. Investigations are currently under way to determine the best methodologies in implementing spatial signal analysis in a production environment.

However, the signatures alone are not conclusive evidence of yield loss. It is the combination of knowledge gained from inline pattern wafer inspection, yield analysis and the identification of the tool signatures that determines when to take corrective action.

Automating the spatial signature analysis, frontside to backside correlation, and signature to tool correlation are the next important steps towards implementing backside inspection into a production environment.

Conclusions

Tight depth of focus requirements in high-end semiconductor manufacturing photolithography leaves little or no room for any localized deviation in the wafer uniformity. At feature sizes of 110 nm and below, any contamination or topography variation on a wafer backside causes process difficulties or even yield loss. This is particularly relevant to the “super flat” 300 mm wafers which have challenging specifications for wafer surface uniformity.

Focusing on 300 mm “super-flat” wafer photolithography, we identified that the backside defect count steadily increases throughout the manufacturing process. There are two major sources of backside defects: defect generation by deposition or furnace processes, and backside contamination by wafer handling. A non-destructive analysis of tool or handler defect signatures on the wafer backsides was facilitated using the BSIM on the Surfscan SP1DLS. A correlation of backside defect data to front side patterned wafer inspection revealed that not all defect issues on a wafer backside are relevant to the photolithographic process. The effect of backside defects is dependent on their position on the wafer, as well as their size, shape and orientation.

The most powerful outcome of backside defect inspection is the identification of spatial defect signatures and their correlation to tool or process fingerprints. The next step is to automate the identification, analysis and correlation of such backside defect signatures to tools and processes.

Acknowledgements

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References

Chris Mack Receives Prestigious SEMI Award

This past December, Semiconductor Equipment and Materials International (SEMI) honored KLA-Tencor’s very own Chris Mack for his significant contributions to the advancement of semiconductor manufacturing technology at the 24th Annual SEMI Dinner and Award Ceremony, held at the Marriott Hotel in Santa Clara, California.

Specifically, Mack was recognized for his development of software programs that have enabled process engineers to increase productivity of the lithography process. His work over the years has driven many changes in the development, production and optimization of photomasks, lithography systems, photoresists and lithography metrology.

The SEMI Award for North America honors individuals who have made significant technical contributions to the semiconductor industry. Past award recipients include Walter Benzing and Mike McNealy for epitaxial silicon deposition; Dan Maydan, Sass Somekh and David Wang for plasma etch; and KLA-Tencor’s own Kenneth Levy for automated photomask inspection.

In addition to his long list of academic credentials, Mack has had a noteworthy career in the microelectronics industry. In 1983, he joined the U.S. Department of Defense, where he began his work in optical lithography research at the DOD’s Microelectronics Research Laboratory. From 1990 to 1991, Mack was on assignment at SEMATECH working in the areas of deep ultraviolet (UV) photoresist characterization and phase-shifting mask optimization. He helped to found FINLE Technologies in 1990, and joined full-time as president and chief technology officer in 1992. Under his stewardship, PROLITH — FINLE’s flagship product — became the de facto industry standard for lithography modeling and data analysis software, and it continues to remain so to this day. When FINLE was acquired by KLA-Tencor in 2000, Mack stayed with the organization, where today he heads KLA-Tencor’s advanced lithography process control development efforts as vice president of lithography technology.

In our next issue of Yield Management Solutions, we’ll sit down with Chris Mack for an exclusive interview to hear about his early years in the semiconductor industry; his experiences as president of FINLE; and how life for him has changed since he transitioned into his current role at KLA-Tencor.
The road to success is paved with new solutions.
Eliminating Buried Yield Killers

e-Beam Inspection: Best Practices for Copper Logic and Foundry Fabs

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Monitoring and eliminating buried electrical defects has become critical for 130 nm copper devices and below. As a result, electron-beam inspection is being widely adopted for development, ramp, and volume production monitoring. In this paper we describe current implementation of e-beam inspection technology for copper logic and foundry fabs, including specific case studies which illustrate the benefits of applying e-beam inspection technology from development through volume production. We also describe methods used to overcome common implementation hurdles. We then pair best practices with new advances in e-beam inspection technology to model the optimal implementation for a hypothetical 20,000 WSPM 300 mm fab.

Introduction

Challenges for production of 130 nm copper (Cu) devices stem from shrinking process windows, complex integration schemes, and the introduction of novel materials. A key issue in manufacturing these devices is that many of the yield-relevant defect types are not detectable using conventional optical inspection tools. Examples include buried Cu via voids, under-etched vias and trenches, and organic residue at the bottom of high aspect ratio dual damascene vias and trenches. E-beam inspection (EBI) can detect these buried electrical defects through the use of voltage contrast (VC) by detecting interruptions in the interconnect path to ground (Figure 1). In VC mode EBI is essentially an inline electrical test on product wafers.

EBI has been widely adopted by leading-edge fabs as an engineering analysis tool during development and ramp. For example, 30 out of 35 Cu fabs worldwide have at least one EBI tool being used in this manner. EBI engineering analysis applications have been documented in the literature by several leading chipmakers, including Toshiba, ST Microelectronics, and TSMC.
Recently, examples of production implementation of e-beam inspection for electrical line monitoring have surfaced, including papers from Motorola, Texas Instruments, Samsung, and Altis. This trend appears to be driven by the recurrence of EBI-unique defects in production, particularly at 130 nm design rules and below. Furthermore, volume production applications are expected to accelerate with the introduction of a new generation of high speed EBI tools. For example, the new KLA-Tencor eS30 is at least two times faster than the previous-generation EBI tool (eS20XP), and can be as much as 12 times faster for certain sample plans. Improvements to production worthiness, defect binning, and ease-of-use have also facilitated implementation in production implementation.

In the following sections we will describe some of the current best practices for EBI implementation in Cu logic and foundry fabs; these will include a benchmarking survey and representative case studies. Finally, we model the ideal fab EBI implementation and determine the corresponding return on investment.

These results are predicated on the performance of the KLA-Tencor eS30, an EBI tool which incorporates KLA-Tencor’s latest technology for development, ramp and volume production applications.

**Best practices for EBI implementation**

To assess best practices we conducted a survey of current EBI utilization within the Cu fab installed base. In the back end of line (BEOL), top applications consistently included the minimum pitch Via 1 module. At Via 1 the most critical defect types were voids, under-etched, over-etched or missing vias, and residue. Inspections for this module are most commonly at Via 1 etch (for photo/etch dominated defectivity) and the subsequent Cu CMP step (Via 1 CMP or M2 CMP for single and dual damascene processes, respectively). Upper metal Cu CMP and via/trench etch inspections are also important despite the looser design rule, due to film thickness variations and integration problems.

The most common EBI point in the front end of line (FEOL) is contact, whether at etch or at tungsten (W) CMP. Driven by shallow junction development, e-beam inspection of the cobalt silicide (CoSi2) or nickel silicide (NiSi) modules are also rapidly becoming critical applications.

Users typically employ higher sensitivity (small pixel) recipes when building the baseline defect Pareto. In development, when defect densities are high, accurate baseline Paretos can be developed by small area inspections (<10 percent of wafer). As systematic problems are resolved and defect densities decrease, more inspection area is needed to attain a statistically valid baseline Pareto.

It is important to note, however, that while the sampling requirements change as a function of the defect density, in almost every case fabs will still sample across the entire wafer to obtain wafer-level defect signatures. Such “full wafer signatures” are obtained by inspecting alternate die rows, using run-time swath skipping, or employing area-accelerated (eD0) test structures such as those described by Weiner et al. A typical eS30 volume production inspection sample plan is shown in Figure 2.

Table 1 summarizes the production line monitor utilization of e-beam
inspection for nine Cu fabs. Line monitor wafer sampling strategies are dependent upon the size of the yield excursion that is to be detected. Many customers who employ critical area models quickly conclude that large-sized chips require more wafer inspection area in order to find smaller excursions. Modeling and empirical fab data indicate that for most volume production monitoring applications sufficient area can be inspected on the eS30 in a one-hour inspection time.

**Faster development and ramp**

EBI enables users to accelerate yield learning during development and ramp by providing an inline measurement of yield-relevant defectivity. In general, the key to successful inline yield learning cycles is a complete understanding of the distribution and frequency of killer defects. Fabs have long used optical inspection tools to develop such understanding for physical defects. However, the transition to damascene Cu structures fundamentally increased the importance of buried electrical defects, such as Cu voids and under-etched vias.

To address this need, most Cu fabs have adopted EBI over the last five years. This technology provides rapid quantification of yield-relevant, electrical defectivity to the engineering teams conducting process window splits and integration studies. In addition, EBI provides faster localization of yield-relevant defect sites. Compared to end-of-line wafer probe and conventional failure analysis, inline EBI can reduce the average time of a learning cycle from weeks to days.

The benefits of this approach are illustrated by Mizuta and Amai. They describe how Toshiba used VC inspection during development and ramp of their 90 nm Cu process. In particular, the authors implemented

**Overcoming post Cu CMP queue time constraints**

Table 1 indicates that the some of the most frequent e-beam inspection points are following Cu CMP. However, many Cu CMP processes impose a queue time constraint to minimize the risk of corrosion. Typically, this constraint is on the order of four to 12 hours from finishing the final post-polish scrub until beginning the etch stop layer (silicon nitride or silicon oxynitride) deposition. Cu fabs employ several strategies to implement post Cu CMP EBI monitors within the imposed cycle time restrictions.

The most common strategy is to implement the post Cu CMP EBI monitor after the nitride cap has been deposited. This is frequently the fab’s preferred approach because it removes the queue time constraint altogether. In some cases, however, this can be a more challenging inspection to perform. Imaging through the nitride cap layer requires a higher than normal landing energy, e.g. 1800eV for a 400Å cap. Furthermore, the nitride cap makes it more difficult to control surface charging; in many cases, some form of active charge control, such as the e-Control™ capability found on the eS25 and eS30, is required.

Another approach is to simply perform the inspection within the allotted queue time. Most production EBI monitors take only about one hour per wafer which, in most cases, will leave sufficient time for other inspection and metrology steps that must also be performed within the queue time. However, the non-steady flow of material through the Cu module may periodically result in a queue at the EBI tool. It then becomes necessary to balance the risk of violating the queue time on some lots against the risk of skipping inspection and missing an excursion.

A third approach is to split inspected wafers from the lot after Cu CMP: the remainder of the lot is capped immediately, while the inspected wafers queue for inspection before being rejoined. The latter method usually requires fab automation typical of advanced 300 mm fabs.
Getting to the defect of interest

Identifying a defect of interest requires both the inspection sensitivity to detect the defect, and the ability to separate it from the many other defect types in a typical inspection result. The latter is particularly important for e-beam inspection (EBI) which, because of its inherently high sensitivity, is able to detect a wide variety of defect types.

KLA-Tencor uses a sequential defect-segregation approach on the eS30 which provides a powerful and flexible combination of imaging configurations and algorithms to quickly highlight defects of interest, suppress nuisance defects, and then bin the defects not of interest. This allows an EBI user to efficiently resolve even the tail of the defect Pareto, and to control the line based on the most relevant yield-impacting contributors.

This method consists of three elements: optimized imaging conditions; nuisance filtering and binning algorithms that take place during the inspection; and post-inspection sorting capability that allows the user to generate the most useful sample plan for high resolution review on the eS30.

![Image](https://via.placeholder.com/150)

A complete EBI defect segregation strategy requires optimized imaging conditions, real-time binning algorithms, and efficient post-inspection review capability.

**Inspection imaging conditions**

The inspection imaging conditions play a critical role in highlighting defects of interest and suppressing noise sources. EBI imaging of defects depends on several variables. For example, the landing energy, beam current, and the field conditions imposed on the wafer surface can turn on and off certain voltage contrast signals by imposing a forward or reverse bias of the structures. Different imaging configurations may be set up as different tests to isolate specific electrical signals.

Landing energy is also important because it affects the relative secondary electron yield and, hence, material contrast of the surface. Furthermore, landing energy can affect the depth of penetration and edge contrast. This ability to tune the material contrast, depth of penetration, and edge contrast allows the user to preferentially detect certain physical defect types.

The authors also demonstrate how inline automatic defect classification (iADC) can eliminate the need for manual review by binning several types of VC and physical defects with greater than 95 percent accuracy and purity. In total, Toshiba reported that EBI enabled them to achieve a faster killer-defect analysis cycle, thereby ramping their 90 nm process about 25 percent faster than their 130 nm process (Figure 3).

**Baseline yield improvement and excursion control in the BEOL**

Buried electrical defects are usually first found during development, but also recur in volume production. The voltage contrast mode available in EBI provides a unique capability to detect
these buried defects on product wafers inline — catching excursions that otherwise would not be found until final test. Many Cu fabs use this e-beam inline electrical inspection to improve baseline yield and to monitor for excursions. For example, Texas Instruments’ 300 mm DMOS6 fab used EBI for volume production of their 130 nm devices, and for prototyping runs of 90 nm devices.

During ramp and early into production, TI DMOS6 noticed yield issues at final test for a DSP product. Optical inline inspections detected defect signatures in the gate loop which were unconfirmed by inline probe, post Metal 2 CMP. When the flagged wafers were inspected using EBI in VC mode post Metal 2 CMP, open contacts were verified. Root cause was determined to be a defect type called poly pillars (Figure 4a), which occurred at a defect density below that which could be resolved by inline probe. After the process was corrected, a lower-cost optical inspection was introduced at sidewall etch to control excursions.

During this investigation a second buried, open-via defect type was discovered using EBI on the same wafers. Via contamination (Figure 4b) was found to be blocking the sputter etch prior to barrier metal deposition, resulting in un-landed vias. This buried defect could not be detected optically, so an EBI inspection point was introduced inline to monitor for open vias. This log-point enabled TI to reduce the magnitude and frequency of open-via excursions and drove a baseline yield improvement of 15 to 20 percent (Figure 5).7

Detection can also be weighted to preferentially detect VC defects by selecting an appropriate pixel size for the inspection. Increasing pixel size reduces the capture of small physical defects while still maintaining a high capture rate for most VC defects (and at very fast inspection speeds). Finally, effective charge control is also necessary to minimize nuisance defects and to allow aggressive thresholds.

The KLA-Tencor eS30, with the widest range of possible imaging configurations, provides users with the unique capability to implement the defect detection scheme most appropriate to the problem at hand.

Run-time algorithms
In some cases, the optimal imaging conditions may not completely suppress nuisance defects. Therefore, a second level of nuisance filtering has been added to the eS30 platform. This filter, known as WISE™ (Wafer Inspection Sensitivity Enhancer), allows the user to reject unwanted defects during inspection.

The remaining defects of interest (i.e., those that are not suppressed by the imaging and pass through the WISE nuisance filter) can then be separated into different bins through the application of iADC, or inline automatic defect classification. iADC operates on the as-detected, multi-pixel image “patches” of the wafer at each defect location. A common eS30 iADC implementation is to bin defects into dark VC, bright VC, multiple VC, and physical defects.

Review sorting algorithms
The final binning operation is to sort the defects using a rules-based approach for selected manual review on the eS30. The majority of Cu fabs perform some manual review on the EBI tool due to the built-in high resolution SEM imaging, state-of-the-art VC imaging capability, and simply the convenience and time savings of not having to move the wafer to a different tool.

The review sorting tools allow the user to apply further granularity to the bins created by iADC. Unlike the run-time algorithms, these are rule-based and so no previous setup is required. This is useful for cases in which defects resemble one another, e.g., single dark VC and small dark particle.

![Figure 4](image1.png)

**Figure 4.** Open contacts and via defects were causing yield problems at TI DMOS6. While the poly pillar defect (a) can be monitored in production using a traditional optical inspection after sidewall etch, the via contamination defect requires EBI monitoring in volume production.7

**Figure 5.** Texas Instruments DMOS6 improved their baseline yield by 15 to 20 percent by using EBI monitoring at Metal 2 CMP. This chart shows the open-via (dark VC) defect density trend over time.7
Baseline yield improvement and excursion control in the FEOL

In addition to the Cu module, non-visual defect detection is also important in the FEOL — particularly for contacts. Altis Semiconductor describes implementation of EBI monitoring to detect excursions inline at contact (W CMP) as part of a comprehensive methodology that also includes EBI monitoring at M1, M2, M3 CMP, CoSi, and Via 1 etch. In one case, SRAM contact post W CMP, several excursions went undetected until final test. Using the voltage contrast capability inherent in EBI to flag open contacts, Altis was able to quickly identify contamination and photo/etch issues. These were later traced to inhomogeneous etch chamber cleaning and micro masking on reticles, respectively. Figure 6 shows the EBI defect yield trend chart for three contact etch chambers. Numerous excursions occurred over the study period. In each case, the inline EBI monitor allowed Altis to detect the excursion and take corrective measures six weeks earlier than if they had relied on final test.

In another case, EDRAM contact post W CMP, failure rates were on average 3.7 times the failure rate of a reference SRAM design. By using EBI monitoring to drive process improvement activities, the EDRAM failure rate was driven down to, on average, 1.2 times the failure rate of the reference SRAM design.

20X return on investment (ROI) for a 20K WSPM, 300 mm fab

Figure 7 depicts the optimal implementation of EBI technology for a typical 300 mm, 20,000 WSPM, sub-130 nm design rule Cu logic fab. In this implementation there are three eS30 EBI tools: one tool for FEOL monitoring (silicide and contact), one tool for BEOL monitoring (Cu CMP and via etch steps), and one tool for engineering analysis. A dedicated engineering analysis tool is necessary to drive baseline yield improvements throughout the technology life-cycle; this tool also would function as a backup for the production tools during maintenance periods.

The model fab results were derived from the benchmarking survey results described in Table 1, case studies and input from KLA-Tencor EBI customers, analysis of excursion data of over 800 lots of material from EBI monitoring at multiple fabs, and performance data from the eS30 e-beam inspection system. Similar examples of the excursion analysis methodology are described in detail by Nurani and Soucek.

The three-year ROI associated with this optimal implementation is...
estimated to exceed 20X (Figure 8). Key assumptions used in the analysis include the following:

- Leading edge design rule with an average selling price (ASP) of $10/die, declining by 10 percent per quarter during yield ramp.
- Nominal time for development (reach 10 percent yield) is 12 months at 1000 WSPM.
- Nominal time for ramp (10 percent to 60 percent yield) is 18 months at 5000 WSPM.
- EBI implementation provides faster learning cycles (inline versus final test) which, in turn, accelerate development and ramp each by six weeks. This 10 percent reduction in time to market is conservative relative to the 25 percent improvement reported by Mizuta (Toshiba).
- EBI monitoring in volume production is assumed to detect one unique excursion every three months at each of the four layers shown in Figure 7. These excursions are further assumed to affect only one of eight lots (one of eight chambers, hoods, etc.), in which the yield on affected wafers drops from 70 percent to 35 percent. Detecting these electrical defects inline instead of at final test is estimated to increase yield by 8 percent. This is a conservative estimate relative to the 15 to 20 percent yield improvement reported by Soucek (Texas Instruments) and other sites that have implemented EBI monitoring in volume production.

This trend will continue to be important going forward. The production ROI illustrates the increasing importance of detecting electrical defect excursions inline.

**Summary**

New technology requirements have led to adoption of e-beam inspection in all phases of the technology cycle — development, ramp and production. A new EBI system (eS30) has been introduced by KLA-Tencor which combines significantly enhanced throughput and sensitivity, with the defect binning and reliability required for production.

Modeling of a 20,000 WSPM logic fab indicates that three high throughput EBI tools provide the optimum ROI for the fab. These results have been validated by several leading chipmakers and serve as a model for new fab space allocation.

Additionally, memory process flow appears to be more susceptible to small physical defects that cannot be detected inline with technologies other than EBI. As a group, memory fabs therefore tend to monitor more for physical defects than Cu fabs and, as a result, use smaller pixel sizes.

More detail on e-beam inspection applications in memory fabs can be found in recent papers from Samsung, ProMOS Technologies, and Macronix for stacked-capacitor DRAM, deep-trench DRAM, and flash memory processes, respectively.

![Figure 8. Impact of optimal EBI implementation on yield curve and return on investment.](image)
References


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Defects occurring within unfilled and filled contacts and vias are among the biggest barriers to production success at 130 nm and below. And the only way to detect them is with dedicated, high-speed electrical line monitoring at every key process step. Introducing the eS30—the industry’s fastest e-beam inspection system. With more than 2x throughput and sensitivity improvements, and the ability to rapidly trend by defect type, the eS30 meets the production requirements for electrical line monitoring. And it maintains the engineering analysis capabilities you need for development and ramp. All in an easy to use, single platform solution. Next stop: eS30. The fastest way to improve and protect your yield.
Q Besides airborne base contamination, can anything else cause T-toping in chemically amplified resists?

A T-topping in positive chemically amplified resists is caused by a reduced level of deblocking (the post-exposure bake induced chemical reaction that enhances resist solubility) at the top of the resist. This reduced deblocking, in turn, is caused by unnaturally low levels of acid, the photochemical product of exposure. So the question is, what can cause acid loss at the top of the resist? Airborne base contaminants, which land on the resist and diffuse into the top portion, can neutralize acid during the delay time between exposure and PEB. The effects of airborne base contamination can be reduced by lowering the levels of base contaminants, reducing the delay time between exposure and PEB, and lowering the diffusivity of the contaminant within the resist. In addition, base additives in the resist can somewhat reduce the magnitude of T-topping whenever the base additive is a stronger base than the contaminant.

Besides airborne contamination, acid evaporation from the top of the resist can produce the same type of T-topping. This occurs when the acid molecule is too small so that its rate of evaporation is not negligible. Most modern resists have large enough acid molecules to avoid this problem. In addition, solvent evaporation during post-apply bake leads to a drier resist film at the top surface. Since solvent content can affect acid diffusivity and therefore the deblocking reaction rate, the result can be a reduced level of deblocking at the top of the resist. While this effect only rarely leads to T-topping, it can enhance the magnitude of T-topping coming from another source.

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Taking Control of the Copper Process at 65 nm

Murali Narasimhan, KLA-Tencor Corporation

The move from aluminum to copper (Cu) interconnects has been driven primarily by the desire for better device performance. However, the transition to Cu created a number of unexpected challenges that slowed the rate of Cu adoption at the 130 nm node and stalled efforts to integrate low-k dielectrics into the interconnect. The transition to the 90 and 65 nm nodes has introduced an entirely new set of challenges. This article explores each of these issues in detail and describes the best-known metrology methods currently available to help IC manufacturers bring the copper process under control at the 65 nm node.

Introduction

With several IC manufacturers now completing the development cycle for their second-generation Cu interconnects for the 90 nm node, process development engineers are now beginning to look at process issues that they are likely to face at 65 nm. What they will find are not incrementally more difficult process integration problems, but rather an entirely new set of challenges that will require the implementation of very specific metrology techniques to keep copper interconnect processing under control. Cu process control issues at the 65 nm node can be broadly classified into five categories: (1) low-k materials; (2) Cu barrier/seed advances; (3) electroplating; (4) Cu chemical mechanical planarization (CMP); and (5) interconnect reliability.

Low-k materials and their process control issues

Back-end-of-line (BEOL) inter-layer dielectrics (ILDs) are evolving into a multi-layer stack of passivation dielectric, etch-stop layers, ILD and inter-metal dielectric, and a potential cap layer in the form of harder silicon carbon nitride (SiCN) to withstand the Cu CMP process. Measuring the film thickness of individual layers within the ILD stacks has proven challenging for some metrology techniques, which have difficulty distinguishing between layers of widely varying thicknesses made from a variety of material types. The presence of under-layer artifacts, especially at higher levels of metallization, also affects the accuracy of film thickness measurements. Simpler optical techniques, such as single- or multiple-angle ellipsometry or reflectometry, often do not provide enough information to separate confusing signals from variations in the multiple layers of interest. Spectroscopic ellipsometry (see sidebar) offers a solution in this case, since ellipsometric information (cos delta and tan psi) is collected simultaneously over 1024 wavelengths. Powerful algorithms then interpret this information to yield the best combination of sensitivity to excursions, robustness to normal process variation, measurement precision, and long-term instrument stability and system-to-system matching (the last two of which are required for production monitoring metrology). Advances in optics technology, modeling algorithms and computational processing have enabled fast and routine measurements of thickness and refractive index of low-k materials with non-homogenous graded compositions, plasma and/or thermal treatment to modify surface and bulk properties, porous low-k materials and multi-layer combinations of these films (Figure 1).

More attention is being placed on the mechanical properties of low-k materials, since the ability of low-k films to withstand Cu CMP processes and stress migration (SM)
after processing is key to achieving optimal chip reliability. Techniques such as nano-indentation and four-point bridge fracture toughness are currently being used for materials characterization and early process development of low-k films. Scientists are also using analytical techniques, such as porosimetric ellipsometry, positron annihilation lifetime spectroscopy (PALS) and x-ray scattering to characterize pore size and distribution — both of which indirectly affect mechanical properties. The need for an inline, non-contact technique for production monitoring of mechanical properties is unclear at this point. However, some early results of applying the photo-acoustic metrology technique to measure Young’s Modulus of low-k films — a key mechanical property parameter — look promising.²

Another emerging process control challenge is the sensitivity of the dielectric constant in low-k materials to post-processing. Temperature cycles and environments with high mechanical, plasma and chemical stresses in post-processing steps can modify and degrade the dielectric constant. Monitoring the dielectric constant is therefore required in production process equipment for 65 nm Cu manufacturing lines. Conventional MOSCAP CV testing can be used for this application, but requires multiple steps to deposit and pattern metal electrodes to form the MOS capacitor on the low-k film being measured. The MOS capacitor must then be probed to obtain the CV curve measurements that must, in turn, be combined with optical film thickness measurements to yield the dielectric constant. The two to three day cycle time involved in making this measurement places significant product wafers at risk, especially given the number of possible process steps that can adversely affect the low-k material. Mercury (Hg) probes have been used to monitor the dielectric constant for many years, but cannot be used inline in an IC fab due to toxicity and contamination concerns.³

Corona oxide semiconductor measurement techniques (see sidebar) offer a solution for monitoring low-k damage by measuring capacitance and trapped charges of a low-k film. A small, precise amount of charge is deposited on the low-k film in the measurement location to form
Spectroscopic Ellipsometry

With increasing complexity of chip fabrication, spectroscopic ellipsometry (SE) has established itself as the technique of choice over the last five years for monitoring thin film processes. This technique relies on the measurement of the optical properties of materials through analysis of reflected, polarized light across a wide spectral range.

SE relies on measurement of optical properties through analysis of polarized light reflected from the sample surface (Figure 1). The incident polarized light is reflected from the sample and passes through an analyzer before striking the detector. In the rotating polarizer version of this technique used in KLA-Tencor systems, the polarization state of the incident light is continuously varied and the detector measures the integrated intensity of the reflected polarized light (for one-eighth of a rotation) at each wavelength. A broadband light source and prism are used to separate the wavelengths of the light incident on the pixels forming the detector array. The integrated intensities form the eight “Sums” corresponding to a complete rotation of the polarizer. The standard ellipsometry parameters $\tan(\psi)$ and $\cos(\Delta)$ can be computed from these eight “Sums” at each wavelength. These quantities are related to the two components $R_p$ and $R_s$ of the reflected polarized light, by the equation:

$$\tan(\psi) \exp(i\Delta) = \frac{R_p}{R_s}$$

where $R_p$ is the electric field reflection coefficient of the component of polarization parallel to the plane of the incident and reflected beams, and $R_s$ is the electric field reflection coefficient of the component perpendicular to that plane. From the above equation, it can then be inferred that $\tan(\psi)$ is the amplitude of the ratio of the $p$- and $s$- components and $\cos(\Delta)$ is the real part of the complex quantity $\exp(i\Delta)$, where $\Delta$ is the phase shift between the $p$- and $s$- components.

Theoretical spectra can be generated based on material models defining the substrate and film stack. A mathematical regression analysis is performed between the measured $\tan(\psi)$-$\cos(\Delta)$ spectra and theoretical computation.

Theoretical spectra includes optical dispersion models (RI as a function of wavelength) and thickness data for the film (or film stack) and the substrate. To ensure accurate and repeatable results, it is vital to have a robust mathematical model of the dispersion. A simple model for the optical dispersion is the harmonic oscillator. This model is based upon the solution for the dipole moment for a harmonically bound electron acted upon by an electric field. Using this model, the dielectric constant is:

$$\varepsilon = 1 + \frac{\sum H_k}{1 - \sum \nu_k H_k}$$

where

$$H_k = \frac{16\pi N_k R_k^3 r_k^3}{(E_{nk} - E^2 + iE_{nk} E)} \varepsilon_{\Phi_k}$$

and $\nu_k$ is the local field correction factor. In the equation for $H_k$, $N_k$ is the density of oscillators for the $k$th oscillator (in units of nm$^{-3}$), $r_k$ is the Rydberg constant ($=13.6058$ eV), $r_0$ is the Bohr radius ($=0.0529177$ nm), $E_{nk}$ is the resonance energy of the $k$th oscillator, $E_{nk}$ is the damping energy of the oscillator, $\Phi_k$ is the phase for the $k$th oscillator and $E$ is the variable energy. The dielectric function is related to the optical constants by:

$$\varepsilon = (\alpha - ik)^2$$

To solve for the parameters in the dispersion model and the film thickness$[4]$, a regression analysis is performed so that the difference between the calculated and measured $\tan(\psi)$-$\cos(\Delta)$ spectra is minimized. Mathematically, the regression is actually performed on the Fourier coefficients corresponding to a complete rotation of the polarizer. The Fourier coefficients are related to $\tan(\psi)$-$\cos(\Delta)$ by:

$$\alpha = \frac{\tan^3\psi - \tan^2 A}{\tan^3\psi + \tan^2 A}$$

and

$$\beta = \frac{2\tan\psi \cos A \tan A}{\tan^3\psi + \tan^2 A}$$

where $A$ is the fixed analyzer transmission axis measured with respect to the $p$-direction polarization angle.

Both the “analyzer” and the rotating polarizer are linear polarizers.

a “virtual electrode.” The surface voltage that is created from this charge is then measured by a Kelvin probe that is positioned at a precise distance above the film. By incrementally depositing more charge and repeating the voltage measurements, a Q-V (charge-voltage) curve is constructed and the relevant properties of the low-k material are extracted. Anneal furnaces, high-density plasma chemical vapor deposition (HDP-CVD) reactors, etch reactors, Cu CMP tools, dry/wet cleaning systems, plasma stripping tools and ashing equipment can all be monitored routinely using this technique (Figure 2).
Corona oxide measurement technology

KLA-Tencor’s Quantox XP dielectric measurement system improves processing capabilities by reducing the time required to gather information for monitoring critical dielectric deposition processes. Quantox employs measurement principles that are highly analogous to MOS C-V electrical testing with the advantages of fast time-to-results and non-contact inline measurement. The Corona-Oxide-Silicon (COS) Quantox system is based on combining three technologies (charged corona, vibrating Kelvin probe, and pulsed light source) to provide comprehensive, fully automated analysis and separation of charge components for characterizing dielectric and semiconductor materials. The charged corona ions provide biasing and emulate the functions of the MOS electrical contact. A graphical description of the components of the Quantox COS systems is shown in the following figure.

The Quantox corona generator produces ions and deposits a precise amount of charge on the surface of the dielectric film to form the “virtual electrode” of a MOS capacitor. The film serves as the dielectric of the MOS capacitor and the wafer as the second electrode. This structure replaces the capacitor structure formed by depositing and patterning a metal electrode in traditional C-V testing. The ions contact the surface with nearly zero kinetic energy, so they do not harm or penetrate the insulating surface. The vibrating Kelvin probe provides capacitive-coupled sensing of the wafer surface potential and functions as a non-intrusive voltmeter with virtually infinite input impedance. The pulsed light source, linked to the Kelvin probe, enables the creation of surface photo-voltage (SPV), and provides measurement of silicon band bending and a direct measurement of $V_{fb}$.

The capacitance of the dielectric film, $C$, is determined from the slope, $dQ/dV$ in the accumulation region of a Q-V curve collected by Quantox. The capacitance is then converted to dielectric constant, $k$, by combining it with optical thickness, $t$, measured using spectroscopic ellipsometry ($k=C*t/\varepsilon_0$). In actual application, some second order corrections can be applied to acquire data to account for semiconductor band bending. The system provides measurement results for production control (dielectric capacitance and leakage) and plasma process monitoring (density of interface traps, surface voltage, and total oxide charge) as well as electrical properties of semiconductor materials.

Advances in Cu barrier seed

While Cu barrier materials at the 130 nm node were generally composed of a single layer of tantalum nitride (TaN) or tantalum (Ta), most IC manufacturers have switched to TaN/Ta bi-layer barriers at the 90 nm node. As a copper barrier material, the Ta/TaN bi-layer barrier offers a number of benefits, such as TaN’s excellent adhesion to silicon dioxide-based ILDs and Ta’s good adhesion to copper.4 For the 65 nm node, ultrathin atomic layer deposition (ALD) barriers composed of either TaN or tungsten nitride (WNx) are being considered. The main attraction with ALD is its ability to deposit highly conformal ultra-thin film layers (down to 10 Å) and provide uniform and conformal step coverage on high aspect ratio vias and trenches. Integration issues, such as adhesion, however, will likely force the industry to continue to use multi-layer barriers for the foreseeable future.

Monitoring Cu barriers poses significant challenges at the 90 nm node and below. Conventional techniques, such as four-point probe sheet resistance or photo-acoustic metrology, no longer work effectively because they are unable to separate the individual layers of the bi-layer barrier. Nor can they measure under Cu seed layers on product wafers. Promising new techniques, such as x-ray reflectivity (XRR), require very complex modeling algorithms and curve fitting. XRR also lacks the small spot size required for product-wafer monitoring.
Barrier composition has also emerged as an important parameter that must be monitored during production. As the barriers become thinner, their composition plays a larger role in their functionality. Changes in composition can affect diffusion properties, interfacial adhesion and film stress — all of which affect SM and electromigration (EM) resistance along with time dependent dielectric breakdown (TDDB) in Cu interconnects. Incorrect barrier composition can also result in high via resistance due to changes in the resistivity and contact resistance of the barrier, thus degrading parametric yield. Conventional metrology techniques do not offer a way to measure composition, and, as a result, IC manufacturers are literally flying blind in production, with respect to controlling the composition of Cu barrier layers. Identifying a method that is capable of monitoring Cu barrier composition inline is therefore essential, as it offers an early warning system for potentially expensive IC reliability failures in the field.

Ultra-thin ALD barriers also lack a reliable product monitoring solution. Current techniques suffer from a number of limitations, including a poor signal-to-noise ratio for measurements on sub-50 Å ALD barrier films. Barrier and seed layer step coverage in trenches and vias continues to be an open challenge for inline metrology techniques. Scatterometry offers a future possibility of monitoring step coverage inline, but this is an issue that currently has no solution.

A promising new technology in the form of electron stimulated x-ray (ESX) metrology (see sidebar) is now available and can be used to measure thickness and composition of Cu barrier/seed layers on product wafers. The technique is derived from electron probe micro-analysis (EPMA), a technique that has been widely used in materials analysis. Advances in electron-beam (e-beam) columns, x-ray detectors and modeling algorithms, combined with fab automation, vacuum wafer handling and pattern recognition, have now made this technique available for fast inline production monitoring in an IC fab (Figure 3).

**Electroplating process control**

Electroplating will continue to be the process of choice for filling trenches and vias at the 65 nm node. Surface topography control during the electroplating process is a key issue, since the additives required to ensure filling often result in so-called “super-filling,” where the thickness of the overburden of Cu is higher on densely patterned areas. These super fillings lead to residual metal due to non-uniform removal during Cu CMP. Voiding of vias and trenches continue to remain an issue due to aging of the electroplating bath and changes in the concentration of additives. The latter is caused by degradation effects of time and temperature on the organic long-chain polymers. In addition, high plating currents can cause edge effects that result in non-uniform thickness at the electrode contact points. These, in turn, can result in residual metal and flaking after CMP.

To adequately characterize Cu thickness inline after electroplating requires a non-contact metrology method that does not cause edge effects. A small spot size is
Opaque film thickness and composition metrology

The MetriX 100 opaque film thickness and composition metrology system is based on electron beam-stimulated X-ray (ESX) technology used in materials analysis for over 50 years. An incident electron beam stimulates x-ray emissions at "characteristic" energies in the films being measured. Beam electrons interact with atoms in a sample through three main processes: Incoming electrons knock tightly bound core electrons out of their shells, and electrons from higher energy levels relax and emit X-rays (source of the ESX signal); freed electrons radiate photons and lose energy (source of the background X-rays); electrons change direction but do not lose energy (source of backscattered electrons).

For high throughput and sensitivity, MetriX 100 uses wavelength dispersive spectrometers (WDS) that are fixed in energy and measure X-ray count rate at fixed points in the spectrum. X-ray emission, absorption, and interaction volume in the film stack being measured is modeled using proprietary algorithms. In order to eliminate instrumental variation and drift, the model accepts as input "k-ratios," which are the count rate from the wafer divided by the count rate from a known standard of the same material stored in the system. The model then calculates film thicknesses and stoichiometry of compound films by iteratively converging to within a pre-set measurement error requirement.

Cu CMP issues and solutions

Cu CMP compatibility has been one of the biggest challenges for low-k materials, and researchers are working to reduce the mechanical stresses generated during Cu CMP by using low down-force and slurry-less processing. Maintaining topographical flatness is a key
requirement for Cu CMP and subsequent lithography steps. Therefore, ensuring uniform polishing and removal rates in order to reduce dishing and erosion — and resultant defectivity — is a significant process control challenge. Atomic force microscopy (AFM) and high-resolution profilometry (HRP) offer a good way to characterize dishing and erosion during process development. Since these techniques are slow and make quasi-contact with the wafer, IC manufacturers are looking for a faster, non-contact method to implement for product wafer monitoring. Both photo-acoustic and ESX techniques offer a way to measure Cu in wide and narrow lines, which allows for the measurement of dishing and erosion (Figure 4). The ESX technique also offers a way to check for residual metal down to 10 Å in thickness in densely patterned areas, where the polish rate can be significantly different from the average rate across the wafer. In addition, the small spot size of the electron beam has also enabled TaN barrier thickness measurement inside wide trenches and power bus line interconnect structures.

**Cu reliability**

Although Cu has been in use in semiconductor fabrication for several years, only now are the reliability failure mechanisms of Cu interconnects being discovered and understood. While the bulk diffusion rate of Cu within itself is low, surface and interfacial diffusion rates of Cu are very high, causing void movement at the interfaces, which in turn lead to EM and SM failure. Bi-layer barriers, which were created for better adhesion, have the additional advantage of improving EM lifetime. However, barrier composition can affect Cu diffusion rates, and thus also impact EM and SM lifetime and TDDB. The different coefficients of thermal expansion between the dielectrics and Cu metal can also lead to higher stress gradients, which exacerbate Cu SM. In addition, vacancies and micro-voids present in the Cu during electroplating fill can coalesce during anneals and chip operating conditions, causing line opens and chip failure.

At the 65 nm node, a variety of engineering solutions are being considered to improve EM and SM lifetime and TDDB of Cu interconnects. Capping layers grown selectively on the Cu surfaces by electro-less plating is one promising method. In this example, a thin layer of cobalt tungsten phosphide (CoWP) or cobalt tungsten...
boride (CoWB) effectively encapsulates the Cu and prevents it from migrating across the dielectric interface and causing leakage and EM failure (Figure 5). Controlling the thickness and composition of the cap layer is critical, since both parameters impact the diffusivity, interfacial adhesion and film stress of the layer. Conventional metrology techniques, such as photo-acoustic or x-ray reflectivity, have difficulty in detecting the interface between the cap layer and the underlying Cu interconnect, and thus cannot measure them effectively. The ESX technique, on the other hand, measures the X-ray emissions from the elemental cobalt (Co), tungsten (W) and phosphorus (P) or boron (B), and can quantify thickness and composition independently. This capability is invaluable for optimizing the capping layer process during process development. It also lends itself in the future for line monitoring applications in production. The small spot size of the electron beam in KLA-Tencor’s MetriX 100 allows the tool to measure thickness and composition on two different features with varying linewidths to optimize process conditions across the die and wafer.

**Conclusion**

The transition to Cu interconnects has proven to be much more difficult than first expected, and numerous challenges remain for the industry as it ramps up to Cu production at 90 nm and begins Cu process development at the 65 nm node. In addition to the increasing number of film layers in ILD stacks that must be monitored, second-generation low-k materials are highly sensitive to post-processing steps, which can degrade dielectric constant. Bi-layer Cu barriers, ALD barriers and other new films introduce new parameters, such as composition, which must be closely monitored in production to minimize the impact of process variations on long-term device reliability as well as short-term yields. Some currently established monitoring methods, as well as a few emerging metrology techniques, have demonstrated the ability to address many of these process control challenges, and show promise in providing the effective copper interconnect control needed at the 65 nm node.

**References**


This article has been adapted from an article originally appearing in the 20th Edition of Semiconductor Fabtech.
Introducing the only inline, non-contact, advanced films metrology tool that gives you the control you need to avoid product failures in the field.

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The Crystal Growth and Reticle Degradation Exposé

Reticle Surface Contaminants and Their Relationship to Sub-pellicle Particle Formation

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Crystal growth and haze formation on reticles continues to be a significant source of concern for the semiconductor industry. Possible sources, causes, and formation mechanisms continue to be investigated. Mask making materials, process residues, reticle containers and fab and or stepper environment can contribute to reticle degradation over time. This paper provides a comprehensive evaluation of various molecular contaminants found on the backside surface of a reticle used in high-volume production. Previously, all or most of the photo-induced contaminants were detected under the pellicle. This particular contamination is a white “haze” detected by pre-exposure inspection using KLA-Tencor TeraStar STARlight™ with Un-patterned Reticle Surface Analysis, (URSA). Chemical analysis was done using time-of-flight secondary ion mass spectroscopy (ToF-SIMS) and Raman spectroscopy.

Introduction

Sub-pellicle reticle contamination was first reported by Grenon et al.¹ as a major concern in high volume semiconductor fabs. Bhattacharyya et al.² identified some of the contaminants as cyanuric acid and ammonium sulfate. Since the initial report, many cases of particle or contamination formation on both 248 nm and 193 nm reticles have been reported. While reported cases of the problem have been increasing as 248 nm lithography becomes more ubiquitous, the introduction of 193 nm lithography in leading-edge fabs has resulted in reports of haze and contamination formation on reticles at greater numbers and at a faster rate.³

As lithographers move to shorter wavelengths, it can be assumed a priori that molecular contaminants in the path of light will be more reactive and possibly effect transmission more radically than at higher wavelengths. While reticle surface contamination has been identified as a significant issue at 157 nm, it is rapidly becoming a critical issue at 248 and 193 nm. It should be noted that the pelliclized reticle structure creates an almost perfect photochemical reaction chamber. Figure 1 shows the basic structure of a pelliclized production reticle.

![Figure 1. Pelliclized reticle structure.](image-url)
The intra-pellicle space can trap molecular contaminants and provide an opportunity for them to react and deposit on reticle and pellicle surfaces. Note that the inner surfaces of the pellicle have several adhesives: a film adhesive that is often cyanoacrylate, the inner frame wall adhesive (IFW), and the frame adhesive. These materials out-gas and can potentially cause crystal formation in the optical path of the reticle. Additionally, surface contaminants on the metal mask and quartz surfaces can out-gas and be trapped in this space.

Because the reticle user identified this problem, this investigation focused on identifying the chemical composition and possible cause(s) of the backside quartz haze. However, it should be noted that identical haze was detected on the inner surface of the reticle storage box, as well as in the intra-pellicle surfaces.

**Defect detection and identification**

*Defect Inspection Method — TeraStar STARlight with URSA*

The reticle analyzed in this study was inspected using the above systems and software options, and was sent for chemical analysis. The URSA option first detected the haze on the backside quartz surface of the reticle. The advantages of this technique are that it provides inspection capability for both surfaces of the pellicle and for the backside surface of the reticle. URSA employs laser scattering illumination and detection technology to find particles, smudges, fingerprints and other handling defects on unpatterned reticle surfaces. STARlight and URSA combined inspection, provides the capability to inspect all the surfaces of a reticle (patterned surface, backside quartz, chromium, and inner and outer surfaces of the pellicle). The features of this inspection technique are:

1. URSA provides a sensitivity of 4 µm (on PSLS) in about two minutes/surface.
2. Darkfield defect preview on pellicles and glass while URSA or STARlight inspections are in progress.

![URSA inspection on STARlight reticle inspection system.](image)

**Figure 2.** URSA inspection on STARlight reticle inspection system.

![Defect map from STARlight URSA inspection — Reticle’s backside quartz surface.](image)

**Figure 3.** Defect map from STARlight URSA inspection — Reticle’s backside quartz surface.

![High magnification image of the haze.](image)

**Figure 4.** High magnification image of the haze.
3. Defect review order from largest to smallest.


5. User adjustable sizing box for defect measurement.


7. View reticle pattern under a defect on pellicle or glass.

These capabilities allowed detection of the contaminants on the reticle prior to any potentially catastrophic use of the reticle in production. Figure 2 provides a brief overview of the basic URSA defect detection system.

**Results of Defect Inspection**
A 6.0 x 6.0 x 0.25 inch pelliclized reticle was inspected on TeraStar STARlight with URSA following extensive exposure in the fab. The results of the inspection indicated a significant level of haze on the backside quartz surface of the reticle. Other defects were evident on the front side of the reticle under the pellicle. For the purposes of this investigation we focused on identifying the composition and magnitude of the haze contamination of the backside of the reticle. Figures 3 through 5 provide data generated during the reticle inspection.

**Defect Identification**
Following defect inspection, the reticle was submitted for chemical analysis. Both Raman spectroscopy and
ToF-SIMS analysis were done on several defective areas of the reticle. Figure 6 provides images of the locations of the analyses.

Raman spectroscopy was accomplished on two of the haze defects that were small amorphous defects in the range of 1.0 µm. These defects were representative of all of the other haze-type defects on the reticle. The Raman spectra were collected using a Renishaw Model Raman spectrometer equipped with a 633 nm laser. The beam size was approximately 1.0 µm in diameter. Background spectra were collected on the quartz surface in order to cancel out the possibility of contamination due to transport and handling during the analysis. The results show the haze to be one compound, ammonium sulfate.4 Figures 7 and 8 show the spectra for the defects analyzed. These spectra are consistent with the spectra previously reported for ammonium sulfate. The possible sources and mechanism of the formation of this contaminant will be discussed later.

In order to verify the elemental composition of the haze defects, we conducted ToF-SIMS analysis on the quartz surface of the backside of the reticle. The instrument used in this work was an ION-TOF, TOF-SIMS IV™ secondary ion mass spectrometer. In this technique, due to the low primary ion fluence, only outer surface monolayers are probed (i.e. a few angstroms). The actual damage to the sample is very low, and thus the method is ‘quasi non-destructive’ or static in nature. This technique provides not only elemental information about the surface, but chemical information as well, in the form of fragmentation patterns of molecular species.

A 15 kV, pulsed 69Ga+ primary ion beam was used for analysis, by impinging upon the sample surface and creating secondary ions in a process known as sputtering. The primary gallium beam was rastered over a 500x500 µm² area in positive secondary ion mode, and 300x300 µm² in negative secondary ion mode. Both positive and negative secondary ions were collected and mass separated via the time-of-flight (TOF) analyser. A traditional first order mass spectrum was then produced by plotting the ion intensity at a particular mass (more specifically, mass to charge ratio, m/e; however, the vast majority of species of interest are singly charged). The
mass range for this work was 0 - 1000 AMU with a maximum of 10,000 possible; however, acquisition time increases with increasing mass range. The nominal resolution approached 10,000 above 200 AMU. The technique has a detection limit approaching PPM levels, depending on the species of interest. As the secondary ion yields are matrix dependent, the technique is not quantitative on an absolute scale, although this may be overcome via the use of appropriate standards.

Figure 9 provides the results of the ToF-SIMS analysis. The intensity scale indicates the relative concentrations of the various ions detected on the surface. The brighter the ToF-SIMS image, the greater the relative concentration of that ion. The figure shows the ions of interest. It is important to note that other significant contaminants were found on the surface and are not shown here. The left side of the figure provides a ToF-SIMS image of the ammonium ions that compose the haze. The remaining images show both the positive ammonium ions and the sulfate ions on the surface.

It is clear from both the Raman spectroscopy and the ToF-SIMS analysis that the haze on the reticle is ammonium sulfate.

**DISCUSSION**

**Chemical Mechanism**

The most common method for reticle cleaning in the photomask industry is the use of sulfuric acid and hydrogen peroxide at elevated temperatures, often followed by a dilute ammonium hydroxide rinse. While the chemistries are similar from mask facility to mask facility, the process recipes can change significantly. The recipes can even vary within a mask facility. This is probably because not all reticles behave in the same manner when exposed. These chemistries can leave residues on all surfaces of the reticle if improperly rinsed; they also react with the quartz surfaces. Some of the more common reactions that can occur are the formation of silicic acid or hydrated silicon dioxide. The ammonium rinse can form ammonium silicate. Figure 10 provides the possible mechanism for the formation of the haze on this reticle. While this may be the most likely cause, it does not obviate other potential causes or mechanisms for haze formation on reticles.

While surface absorbed ammonium ions are the most probable source of the ammonium ions; other environmental sources of ammonium ions could cause the formation of the ammonium sulfate. However, in most fabs where chemically amplified resists are used, activated charcoal filters are used to filter out ammonia and ammonium ions; therefore, environmentally deposited...
ammonium ions are an unlikely source. Sulfate ions are not labile (likely to easily undergo chemical change), therefore it is mostly probable that these ions were on the reticle as a cleaning process residue. Other possible sources of sulfate ions could be environmental, however unlikely this is. Unpublished results have shown high concentrations of sulfate ions on all mask surfaces following mask cleaning.

**Exposure Conditions for Haze Formation**

While exposure conditions for particle and haze formation can vary significantly from fab to fab and from reticle to reticle, exposure conditions under which the haze formed on the reticles in this paper are well understood. Figure 11 provides data for several reticles that have shown haze formation on both the backside, as well as the chromium side of the reticles.

The above chart indicates that the formation of contamination defects is linear for 248 nm exposure and almost exponential with dose for 193 nm. For this reason reticles exposed at 193 nm provide a greater risk for catastrophic failure in the fab; hence, they should be inspected at a greater frequency.

**Conclusions**

Crystal growth and haze formation on reticles continues to be a significant source of concern for the semiconductor industry. Possible sources, causes and formation mechanisms continue to be investigated. Mask making materials, process residues, reticle containers and fab and or stepper environment can contribute to reticle degradation over time. In the case of this study, we feel that the most probable source of the haze formation was residues left on the reticle during the fabrication process.

Backside glass haze can effect overall mask transmission and thus can cause a dose shift on the wafer. A dose shift can be serious because most low k₁ processes run with a very small process window and therefore a small dose shift can create a serious yield issue. The backside haze can be easily and reliably detected by Starlight URSA inspection. An ideal quality control approach is to detect any possible reticle degradation prior to any catastrophic failure in the fab. This can best be accomplished by re-inspecting reticles prior to exposure. It is recommended that a carefully-developed reticle inspection strategy be implemented to minimize mean-time to detect defect growth. This is best done by understanding the cumulative dose seen by the reticle and correlating it with the first detection of reticle degradation. These values will vary as a function of wavelength and exposure dose in the fab. As a result, each fab should develop specific inspection and re-qualification plans for reticle.

The rate of contamination formation on these reticles was significantly faster at 193 nm exposure than at 248 nm, hence a greater inspection or re-qualification frequency would be recommended for 193 nm lithography.

**Reference**


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"Remember that 'nuisance' reticle defect everyone ignored?"

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Implementation of High Resolution Reticle Inspection in Wafer Fabs

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Many advanced wafer fabs are currently fabricating devices with 130 nm or smaller design rules. To meet the challenges at these sub-wavelength technology nodes, fabs are using a variety of resolution enhancement techniques (RETs) in lithography and exploring new methods of processing, inspecting and requalifying photomasks. The acceleration of the lithography roadmap imposes more stringent requirements on mask qualification and requalification to ensure that device yields are not compromised: mask inspection tools of today need to find smaller defects on reticles against considerably more complicated patterns or tighter critical dimensions (CDs). In this paper we describe the early stages of implementation and proliferation of advanced reticle inspection tools at high volume manufacturing wafer fabs. We describe the tools and procedure used to streamline reticle requalification at the fabs and improve the feedback loop between the fabs and the mask shop.

Introduction

This paper describes an SL3UV inspection tool-based infrastructure for contamination inspection of reticles in wafer fabs. This tool scans the patterned surface of the reticle using a 364 nm laser in simultaneous transmitted and reflected (STARlight™) mode to detect defects. Such defects include particle contaminants, stains, scratches, crystal growth or also certain kinds of pattern defects/irregularities. Central to the defect detection methodology of these requalification tools is the procedure of STARlight calibration. During this procedure, the tool acquires images by sampling various geometries on the reticle and constructs a database of their transmitted and reflected (T/R) light properties. Then, during inspection, the tool scans the reticle, one swath at a time, and the algorithms compare the digitized T/R measurements at each point on the reticle against the previously constructed T/R database to identify outliers or defects. Unlike pattern defect tools, which use a die-to-die or die-to-database comparison, the SL3UV tool does not require a reference comparison image to identify defects.

The STARlight tools have a sensitivity limit of ~0.18 µm at the 0.25 µm pixel (P250), as measured on polystyrene latex spheres (PSLs). The tools can also be equipped with the unpatterned reticle surface analysis (URSA) option, which allows quick inspection of the chrome-side pellicle, the back glass surface and, if present, a back glass pellicle. URSA is a darkfield (off-axis illumination) inspection system which uses 690 nm laser light to look for particles, scratches or pellicle tears down to a resolution limit of ~4 µm. Figure 1 on the following page shows a schematic of an SL3UV system with STARlight and URSA.

In the following sections we describe the early stages of implementation of the SL3UV inspection tools at high volume manufacturing wafer fabs. First, we discuss the reticle qualification and requalification methodology, followed by a section which compares the differences and improvements of using the SL3UV tool in a wafer fab, as compared with previous methods of reticle verification. Then, we present some data illustrating the success of these tools for reticle requalification.
Reticle Inspection Methodology

The SL3UV reticle inspection tools in the fabs as well as at Intel Mask Operations (IMO) are connected to a central data server via Ethernet as shown in Figure 2. The data servers (KLA 9Xi) function as the central repository for inspection reports and also communicate with various reticle repair tools. The primary data server is where inspection reports and recipes for outgoing reticles are stored. Each tool in the fab can download the inspection report and/or recipe from the primary data server. The connectivity of multiple inspection tools to the primary data server facilitates the process of reticle IQC (incoming quality control) and reticle evaluation.

The reticle management flow is illustrated in Figure 3. All reticles are inspected at the mask house in a final/outgoing contamination inspection, and the recipes and inspection reports are stored on the primary data server. Upon receipt at the fab, when a reticle is loaded into the tool for inspection, the tool automatically identifies and reads the barcode on the reticle and retrieves the outgoing inspection report from the primary data server. The fab engineer then reviews the outgoing inspection report and uses the inspection report (recipe) to perform an incoming inspection on the reticle, to identify any new defects added since the final inspection. Defect-free plates are sent to the exposure tools for printing wafers. If any new defects are found that fail the defect specifications, the reticle is shipped back to IMO for cleaning and re-pelliclization. In the case of questionable defects, images of the defects are stored in the inspection report during defect review and classification. The inspection reports are then saved on the primary data server, and can be accessed for evaluation by an engineer at IMO. The decision of whether to return the reticle to IMO, or not, can thus be made quickly and more efficiently.
Generally, for each reticle loaded into the tool for incoming inspection, three surfaces are inspected: the patterned chrome surface, the chrome pellicle and the back glass surface. Depending on the process layer, the reticles are inspected at the 0.25 µm pixel (P250) or the 0.375 µm pixel (P375). The average inspection process at P375 pixel takes about 65 minutes: 45 minutes for the chrome surface STARlight inspection, five minutes for the URSA glass and pellicle inspections and 15 minutes for setup and review. At P250, the complete inspection takes about two hours. For each pixel size, the inspection times can be reduced by about 40 percent by using the Fastscan mode albeit at the cost of somewhat reduced sensitivity. Requalification is done after some pre-determined number of reticle loads and, like the incoming inspection, also includes an inspection of all three surfaces. Depending on device layer and associated defect specification, the operator identifies all defects that violate the given defect specification for the surface that is being inspected. These defects are dispositioned appropriately following the flow defined in Figure 3.

**Reticle inspection versus print test**

Before implementation of the UV inspection tool, legacy inspection tools with lower defect sensitivity were used to qualify all reticles for the current process. To reduce the number of false defects on the tightest layers of the processes, the previous tools were desensitized to catch only defects larger than 3 µm. This was necessary because diffraction of the blue light on the fine lines of the critical layers caused false positive signals. The pellicle can prevent most of the sub-micron sized particles/contaminants from getting on the chrome surface, keeping the probability of a repeating bad die event low. However, if such an event were to happen, the risk to wafer yield would be extremely high. Therefore, to further curb the risk of repeating bad die events, the fabs implemented print tests. First, a test wafer was printed with the reticle that needed inspection. Then the wafer was inspected on a brightfield inspection tool for repeating bad die defects. The tests consumed stepper and metrology tool time as well as engineer time for writing the recipes. Additionally, the print test was only possible to do on multi-die reticles.

The introduction of the higher resolution reticle inspection tools in the fabs has provided a number of improvements over the previous reticle qualification process (lower resolution inspection, followed by a wafer print test) and eliminated the need for print test verification. Some of the improvements/advantages with the new qualification methodology are:

- **Lower cost of reticle inspection:** A wafer print test consumes about 15 minutes of scanner and track time as well as operator time. Such tools are kept fully loaded, therefore 15 minutes worth of opportunity cost from product that is not produced, is lost as well. The wafer is inspected on a die-to-die inspection tool with high sensitivity settings. This consumes about an hour of tool time and a half an hour of operator time. Assuming a wafer average selling price of $2800, a throughput of 40 wafers per hour and 10 layers per device yields a lost opportunity cost of $2800 per mask per 15 minutes of scanner time. Further, assuming a depreciation rate of 20 percent per year for litho equipment, the total cost associated with performing a single print test verification is about $3000.a, b On the other hand a full plate reticle inspection of the patterned surface, as well as the backside glass and pellicle takes about 65 minutes at the P375 inspection pixel and about two hours at the P250 pixel. If all inspections are done at the smaller pixel size (about 1.5 hours of machine time and about 30 minutes of dedicated operator time for setting up the plate and reviewing the defects), and we use similar numbers as before for the rate of depreciation of the tool and hourly operator costs, the cost of a single reticle inspection is about $150. Considerable cost savings are, therefore, realized if reticle inspection can eliminate or reduce the need for print test verification.

- **Increased inspection automation:** The STARlight tool inspections can be completed with little user intervention. The tool will load, align, calibrate, inspect, and unload automatically. When the inspection is completed, the technician can go back to review and disposition the inspection. In the previous methodology of reticle qualification, every reticle was run through a two step process upon initial receipt: A coarse reticle inspection, sensitivity about 3 µm, followed by a print test. This two-step process involved significantly different tools as well as required multiple engineer support. The print tests were especially demanding because they required expensive lithography tool time. An engineer was required to write a first

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a These numbers are conservative averages taken from the literature. They do not represent specific Intel products.
b Representative cost of a state-of-the-art litho cluster (scanner + track) is assumed to be $1.4M, approx. 4x the cost of an S3UV inspection tool. The costs associated with the wafer inspection tool required for the print test are ignored here.
level job for the tools. After a wafer was exposed, a second engineer was required to write a job for the die-to-die wafer inspection tool. With the SL3UVs this process has been streamlined to a single inspection requiring a single engineer/operator.

- **Standardized defect classification and memory:** One inherent disadvantage of conventional reticle inspection tools over a print test methodology is the fact that reticle inspection tools may detect some fraction of defects that are unlikely to print on the wafer (or are smaller than the defect spec for a given layer/node). To save time reviewing defects that have previously been reviewed and passed, the SL3UV’s have a “Display New Defects” option. This option allows the operator to define a particular inspection as the baseline inspection. Generally this baseline inspection is one where the operator has carefully reviewed all of the relevant defects. Thereafter, every subsequent inspection of the reticle in the New Defects mode compares each defect found in the current inspection with the defect list in the baseline inspection, and reports only new defects. Using this feature increases the efficiency when a large reticle throughput is required and facilitates operator multitasking, i.e. handling of multiple tools.

- **Batch processing:** The SL3UV tools can also be configured with autoloader capability to handle multiple reticles. The software allows the operator to queue up multiple inspections with different recipes, cycling through one or more of the ten slots. When the autoloader queue is completed, the operator can review all the inspections together at once. The total defect count, which can include some nuisance or sub-spec defects, can vary considerably depending upon the reticle. However in almost every case there is a significant decrease in review time in the New Defects mode.

- **Increased sensitivity on tighter layers:** The STARlight tools have a PSL sensitivity of approximately 180 nm at P250 and 269 nm at P375. Defects of this size can be reliably detected on the patterned chrome surface without being overwhelmed by “false” defects due to scattering or diffraction effects.

- **Imaging microscope integration and enhanced features:** The integrated on-the-tool review capabilities of the SL3UV allow for rapid review and dispositioning of all the defects within a few minutes following an inspection. The default review screen uses a 150 nm pixel size for live image review and offers the option to apply an additional 4x zoom (electronic), as well as a user-defined bounding box to size the defect.

The use of the SL3UV tool has been especially useful in the introduction of new products to the factory and in the rush to bring them to the market. The introduction of these new products to the factory can continue without extra delays. Previously, the arrival and qualification of reticles would be the gating factor for delivery of new products. The first lots of the product would be delayed by the inspection and qualification times of the reticles that were received “just in time.” New reticles would first need to be inspected on the legacy reticle inspection tool, wait for an engineer to write a scanner job, and make a first level print on a test wafer. The wafer would then be sent to the die-to-die inspection tool where a second engineer would create a recipe and inspect the wafer. If the entire process went smoothly the reticle would be qualified about 12-18 hours after it was received at the factory. By using the SL3UV tool, new reticles are qualified immediately upon receipt (i.e. within about two hours) and sent into production right away.

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**Figure 4.** New Defect counts normalized by the total defect counts for five product reticles.
Reticle requalification results

As illustrated earlier (Figure 3) the SL3UV tools at IMO and the fabs are connected to a central data server. The decision of whether to return the reticle to IMO, or not, can thus be made quickly and more efficiently. Figure 5 shows the proportion of total reticles shipped that were returned to the mask shop for “invalid” reasons over the period 2001-2002. This period also coincides with the introduction and proliferation of SL3UV tools into the fabs. The solid line in the figure is a linear fit to the data over the two-year period. Though fluctuations in the return rate from one quarter to another can be attributed to a variety of factors, the trend does show a gradual improvement (decrease) in the percentage of invalid returns. We attribute this improvement in part to the improved communication/flow between the mask shop and the fabs.

Finally, we present an example where a potential killer defect was identified and caught by the SL3UV, and the mask was appropriately handled with minimal disruption to the fab or IMO. Figure 6 shows the example of a “damaged upon use” mask site that was caught using the SL3UV. This defect was initially missed during the reticle inspection with the 0.375 µm pixel, but was detected by the wafer inspection tool (KLA-Tencor 2135) during print test, as shown in Figure 6(b). However, identification of the layer containing the defect from the wafer images was found to be very difficult due to the defect geometry and its location.

Once the suspect mask layer was identified, the reticle was re-inspected at tighter sensitivity on the SL3UV (with the 0.25 µm pixel) and the defect was detected with a 100 percent capture rate. A saved image of the defect was then reviewed electronically with IMO engineers, and the mask was removed from the production line. This entire problem was resolved without shipping the reticle back to IMO.
Whereas the above event illustrates the value of having an effective reticle management system, it also points out the importance of selection of the inspection pixel on the SL3UV system. As with any inspection system, defect sensitivity of the tool depends upon the feature size and half pitch on the reticle. For optimal performance the pixel size should be selected such that the background pattern is well sampled. This is specified as

\[
\text{Inspection Pixel Size} \leq \frac{1}{2} \times \text{Primary Feature Linewidth}
\]

For the SL3UV the required minimum primary feature linewidth is 750 nm for the P375 inspection pixel and 500 nm for the P250 inspection pixel.

Conclusions

The SL3UV tools, connected to a central data server at Intel Mask Operations, are being used to provide an integrated solution for reticle management at Intel fabs. Use of these tools not only provides a significant relief from the high opportunity cost of using steppers for print test verification, but also streamlines the communication between the fabs and the mask shop. The automation and “new defects” features on these tools enable faster incoming qualification (IQC), particularly for new product reticles. Shorter IQC and requalification times, and a steady decline of reticle returns for nuisance/invalid reasons from the wafer fabs to the mask shop, have resulted in increased productivity at both ends of the line.

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Introduction

Shrinking design rules and low k₁ lithography bring an increased sensitivity to reticle defects during the wafer printing process.¹ A single, printable reticle defect that destroys the chip in which it resides can reduce the yield of a fab area by 25 percent in the case of a four die reticle, and up to 100 percent in the case of a single die reticle. The increase in wafer cost, particularly at 300 mm, intensifies the adverse financial impact of such yield losses. Great care is taken by wafer lithographers to interact with reticle suppliers to generate defect specifications which will prevent this occurrence. Indeed, much of the expertise of a modern mask shop centers on the prevention, detection and repair of these defects.

The task of inspection, however, does not end when a reticle is delivered to the lithographer and placed production. In the first place, many wafer lithographers prefer to do an incoming quality control (IQC) on the reticle to assure the reticle manufacturer has met the specifications. Second, a large body of evidence exists² showing that defects can actually grow under the pellicle of a once defect-free reticle, causing a printable, and in some unfortunate cases, a killer defect. The defects are particles, crystal growth, and electrostatic damage (ESD) to name a few (Figure 1). The ultimate cost of such defects has been known to run into the hundreds of millions of dollars per incident. In cases where the proper reticle inspection equipment and a rigorous procedure for its use are in place, the incidence of catastrophic reticle defects has been reduced, effectively, to zero.

Clearly, wafer lithographers must enter the world of reticle defect inspection.

The purpose of this article is to assist the user in selecting the best reticle inspection tool for IQC and reticle qualification at each wafer fab site. First, it is important to establish the goals of the inspection program with respect to application, defect size and design rule. Some goal setting considerations will be presented. Second, and most important, it is essential to select a suite of test reticles that will thoroughly evaluate the tools under consideration with respect to sensitivity and inspectability, but also from the standpoint of ease and speed of operation. Some commonly available test reticles will be described. Next the actual evaluation process will be discussed, emphasizing hands-on operation of
Goals

The first goal to follow is to look beyond the specification sheet provided by the inspection system vendor. These specifications are provided to set a predetermined performance level for inspection system acceptance. The only way to determine actual performance is to allow for a thorough system capability evaluation.

One of the best sources of information on setting goals for an inspection program is the reticle manufacturer. Reticule inspection engineers spend much of their time evaluating reticle inspection equipment and deciding which is best for each inspection challenge. Most are willing to share this wisdom with good customers.

Because of the high cost of the reticle inspection equipment, the program goals should be based on at least the next two generations of product introductions. If 130 nm is in current wafer production, the reticle inspection equipment typically desired would be capable of also doing pilot reticles at 90 nm. Once this decision is made, the International Technology Roadmap for Semiconductors (ITRS) will yield a fairly simple table of requirements for defect size sensitivity, pattern inspectability (i.e. the minimum pattern size which can be inspected without too many false defects). See Table 1.

It is important to decide on the specific applications intended so the correct equipment can be determined. Table 2 shows several such choices.

If IQC is intended, the inspection system suite should match that of the reticle manufacturer, providing full die-to-die and/or die-to-database capabilities for detection of hard pattern defects. For reticle re-qualification, simultaneous transmitted and reflected light systems are recommended. They are fast and highly sensitive. These strategies are outlined in Table 1.

In addition to these plans, a rigorous operational regime must be implemented to make most effective use of the equipment. In addition to operating procedures for the equipment, such a plan should include frequency of inspection and defect size requirements for each type of reticle.

Part of the equipment selection plan should include time and resources to travel to the inspection system manufacturer and do hands on demonstrations of the equipment. Only then is it possible to observe the ease

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Figure 1. Photographs of reticle defects which have been created under pellicles after reticle manufacture and may cause wafer damage.

Table 1. Defect detection requirements according to the ITRS Roadmap.

<table>
<thead>
<tr>
<th>Node</th>
<th>Minimum 4X Geometry (line space)</th>
<th>Minimum 4X OPC feature</th>
<th>Printable defect @ 4X</th>
</tr>
</thead>
<tbody>
<tr>
<td>130 nm</td>
<td>360 nm</td>
<td>180 nm</td>
<td>104 nm</td>
</tr>
<tr>
<td>115 nm</td>
<td>300 nm</td>
<td>150 nm</td>
<td>90 nm</td>
</tr>
<tr>
<td>90 nm</td>
<td>260 nm</td>
<td>130 nm</td>
<td>80 nm</td>
</tr>
</tbody>
</table>

Table 2. Recommended equipment for different inspection applications.

<table>
<thead>
<tr>
<th>Application</th>
<th>Type of defect to be found</th>
<th>Inspection technology</th>
<th>Specific system Names (KLA-Tencor products)</th>
</tr>
</thead>
<tbody>
<tr>
<td>IQC</td>
<td>Pattern defects and contamination</td>
<td>Die to database + die to die</td>
<td>TeraScan and TeraStar</td>
</tr>
<tr>
<td>Reticle Re-qualification</td>
<td>Contamination only</td>
<td>Transmitted &amp; reflected light</td>
<td>TeraSTAR with STARlight inspection</td>
</tr>
</tbody>
</table>
of system operation, the ease of defect classification and the absence of small sensitivity-improving adjustments during the inspection of test reticles. Resources for test reticle acquisition should also be anticipated.

**Selecting the test reticle**

A common mistake in the selection of a test reticle is to present to the equipment vendor a single reticle, frequently the very one which has a printable defect that caused a recent yield loss. Most probably, this defect will be easily found by all types of reticle inspection equipment. Finding this single large defect is no guarantee that the system will also find much smaller and more subtle defects which will also cause killer defects on wafers. It is far better to use a suite of reticles (including the problem reticle) which will exercise all areas of equipment performance.

Many such reticles have been developed and used by reticle and equipment manufacturers for inspection system purchase decisions. Table 3 shows some of these designs and states their advantages and disadvantages.

**Selection criteria for test reticles**

**Defects in “real life” geometries** — It is beneficial for test reticles to simulate actual device geometries where possible. This forces the system to find defects in environments similar to those it will encounter in a actual product reticle. Naturally, the test reticle may not exactly match the designs being inspected but they should present a typical situation.

**Redundant defects** — For assessing sensitivity, it is important to have multiple identical defects. This will allow rapid assessment of sensitivity and easy location of problem defects. At least three identical defects in identical surroundings for each defect type and size increment is recommended.

**Small defect incrementing** — Most inspection systems will find a 300 nm defect and will not find a 30 nm defect. The way to truly differentiate between systems is to use a test reticle with small defect increments so the true sensitivity differences can be demonstrated. A 15 nm increment is recommended.

**Testing false defect detection capability** — The layout of a test reticle is very important. Newer test reticle designs allow the comparison of two non-defective die for the purpose of determining the occurrence of false defect detections. System vendors are then forced to demonstrate sensitivity and false defect performance with the same system settings.

**No special sensitivity options activated** — Some inspection systems have so called “cell to cell” mode which is automatically activated when repeating identical cells are detected. Sensitivity is increased in these areas. Since uniform sensitivity over the entire reticle is the real life requirement, a test reticle should be used that prohibits “cell to cell” mode. This is accomplished by randomly varying the cell size in which a programmed defect appears.

**Highest quality manufacturing** — It is vital that the test reticles be made by the most exacting reticle manufacturing techniques. Common reticle errors such as stripe butting errors and CD variations will be detected by the most advanced inspection systems causing the system to be less sensitive to the programmed defects. Under these conditions, the comparative results will be clouded. The system manufacturer should either have plates which are satisfactory or provide information on where they can be purchased.

An ideal reticle suite might consist of the following:

- **REYCON 2** — for defects in random geometry and testing of false defect detection capability
- **REYCON 3** — for defects in contacts and testing of false defect detection capability
- **CETUS** — for defects in contacts measured by transmitted flux
- **UIS** — for inspectability of simulated patterns which cause problems for reticle inspection

**Running the evaluation**

As stated earlier, it is imperative to conduct a defect inspection equipment evaluation in person and to observe, first hand, the operation of the inspection system. Most inspection system vendors will accommodate this requirement. This is the best way to observe not only the system operation but to determine the capability of the manufacturer to manufacture systems reliably and to support them in the field. Typically three to five days will be required for this activity.

**Items to accomplish during visit**

**System overview** — The reticle inspection system
vendor should present information on how the system works and how it is operated. This should include information on the number of systems in the field, percentage uptime achieved, field service strength, upgrade paths and roadmaps for future technology improvements.

**System setup** — The steps required to set up the system to run the test plates should be thoroughly explained. This should include a discussion on all of the sensitivity and inspectability options available and the way these options are stated on the inspection report.

**System operation**

**Scanning** — The plates should be set up and scanned by the system. It is useful to note the time required to start and complete this operation as a guide to what throughput can be achieved. Typically 10 scans should be made to accurately demonstrate the system’s capability.

**Classification** — This very critical step can only be evaluated first hand. The system optics must be good enough to do accurate and fast classification of the defect sites established during scanning. If it is hard to see the defects, an operator might either misclassify a defect or ignore it altogether. This misclassification could cause a real defect to be classified as a false defect, resulting in a defective reticle being used on wafers.

**Reporting** — The system should be capable of manipulating data and generating useful accurate reports which contain all of the system parameters used in the inspection.

The evaluation event should leave the prospective user with the feeling that the system will do the job and that the company behind the system can keep it running and upgrade it as required by future technology improvements.

### Table 3: Available test reticles for inspection equipment evaluation in order of technology.

<table>
<thead>
<tr>
<th>Name/Source</th>
<th>Pattern</th>
<th>Description</th>
<th>Advantage</th>
<th>Disadvantage</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPICA</td>
<td>![Image]</td>
<td>Defects in simulated device geometry at 15 nm increments</td>
<td>Applicable for most advanced nodes</td>
<td>None</td>
</tr>
<tr>
<td>KLA-Tencor</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>CETUS</td>
<td>![Image]</td>
<td>Defects in contacts from 1% to 30% flux increment</td>
<td>Excellent for difficult contact defects. Good incrementing</td>
<td>None</td>
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<td>KLA-Tencor</td>
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<tr>
<td>Orion</td>
<td>![Image]</td>
<td>PSL spheres down to 80 nm</td>
<td>Only true contamination standard</td>
<td>Defect location not known without first inspecting reticle</td>
</tr>
<tr>
<td>KLA-Tencor</td>
<td></td>
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<tr>
<td>SEMI</td>
<td>![Image]</td>
<td>Programmed defect test masks for lines and spaces, and contact holes</td>
<td>Universal, Impartial</td>
<td>Available for larger features</td>
</tr>
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<td></td>
<td></td>
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</tr>
<tr>
<td>Reycons 2</td>
<td>![Image]</td>
<td>Defects in simulated device geometry down to 600 nm size and 30 nm increment</td>
<td>Excellent for “Real Life” test. Good incrementing</td>
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<tr>
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<tr>
<td>Reycons 3</td>
<td>![Image]</td>
<td>Defects in simulated contacts down to 600 nm and 30 nm increment</td>
<td>Excellent for difficult contact defects</td>
<td>None</td>
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<tr>
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</tr>
<tr>
<td>Verimask</td>
<td>![Image]</td>
<td>Many defect types with defect sizes down to 54 nm at 54 nm increment</td>
<td>Universally used</td>
<td>Equipment can be tuned to detect these defects only</td>
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Data reduction
A typical defect inspection event, such as the evaluation of a test reticle, produces a large amount of data consisting of system set up information followed by a complete listing of all of the defects found. To create useful information from this report, the defect coordinates must be compared with the known locations of programmed defects on the test reticle. Looking up the size of the programmed defect at that location makes it possible to determine the detection sensitivity of the system (i.e. what was the smallest defect of each type that was found).

This can involve a massive amount of work unless the process is automated by the equipment vendor. It is important to establish that this capability exists before beginning the evaluation.

Finally, for the data to be useful, it must be plotted on a chart similar to Figure 2. Here the detection requirement for the planned nodes is compared with the detection capability of the system for each of the defect types on the test reticle. Note in the example shown that, while there were variations in the sensitivity of the system to different kinds of defects, all were detected 100 percent of the time (10 inspections were made) down to the 100 nm level. This indicates that the system is satisfactory for the 130 nm node. Testing of this type on multiple test reticles will guarantee that the inspection system will satisfy the requirements for IQC and reticle qualification.

Final decision
When the testing is finished and all the reports are complete, a decision about system purchase can be made. The overriding concern is to pick a system which has sufficient defect detection capability to find printable defects that will cause the loss of wafers and to give early warning to degradation of reticle quality due to progressive defects like particles, crystal growth, and ESD. All other criteria are secondary to this. The cost of a wafer yield mysteriously dropping to 75 percent or 33 percent, or even 0 percent, is just too high to compromise on this vital parameter. Defect detection capability must be sufficient for the generation of product being run now as well as for one or two planned future generations.

When two systems compare favorably from this standpoint, the other points such as company stability, system extendability, and ease of system operation should be compared.

Reticle defects generated after pelliclization which affect more than ten lots are being reported at higher rates each year. The financial impact of these events is huge. Wafer manufacturers who have taken the time to select the proper reticle inspection equipment have reduced their losses from post fabrication reticle defects to near zero.

References
**Introduction**

Haze, the low frequency signal of light scattering on unpatterned wafers, is already accessible on the Surfscan SP1 in most fabs and contains very useful surface information. It can be used as a proxy for other metrology tools to measure thickness, reflectivity, roughness, defects, and can be integrated in SPC tests for equipment monitoring. When combined with defect measurements, it provides additional wafer surface information unrevealed by defect monitoring alone.

**Light scattering tools**

In this study, we focus on the use of the KLA-Tencor Surfscan SP1™ unpatterned wafer inspection tool to extract the haze signal from the tool’s scattered signal. The wafer is illuminated by a laser, with a beam either normal to the wafer surface or oblique (70° to the normal). The scattered light, coming from different defects as well as the background of the wafer surface, is collected by two separate channels. The low frequency component of the signal of these channels is given as the haze signal, expressed as scattering power fraction per area of detector to the total incident power (ppm/Star radial).

**Haze reference wafers**

To validate the haze signal, a set of standard calibration wafers was developed on a SEZ spin processor. These wafers, which remained stable over time and were
cleanable, allowed us to evaluate tool stability and to perform tool-to-tool comparisons for different light scattering tools. As shown in Figure 2, a set of different standard haze wafers is used as a reference to monitor the haze signal over time for the different channels of the SP1 (in this case the dark field wide oblique channel). A good reference is necessary, since a shift in haze value was observed after a technical intervention with the inspection tool.

The creation of these different haze standards, using varying surface roughnesses, allows us to link AFM measurements (RMS [nm]) with haze (ppm/Sr). Figure 3 demonstrates that most of the SP1 channels are very sensitive for changes in roughness, especially for wafers with a particular frequency diagram.

Fluctuations in process parameters, such as temperature and pressure, often cause deviations in poly grain size during the poly gate process, one of the most critical steps in DRAM device production. These deviations can lead to lower-binning products or device failures. One example of haze monitoring of grain size variation for a rugged poly process is shown below:

The haze signal monitoring capability on KLA-Tencor’s Surfscan SP1 DLS unpatterned wafer inspection tool can be used in many ways: as a measure of nano-sized particles (<50 nm) density, surface roughness of metallic layers, grain size variations, and to inspect small process defects induced in CMP and deposition processes. The new MX 4.0 haze normalization option further allows normalized haze data to be used for thorough monitoring of process excursions in wafer and IC fabs as the tool inspects wafers and captures defects.

Monitoring with haze

Fluctuations in process parameters, such as temperature and pressure, often cause deviations in poly grain size during the poly gate process, one of the most critical steps in DRAM device production. These deviations can lead to lower-binning products or device failures. One example of haze monitoring of grain size variation for a rugged poly process is shown below:

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The creation of these standard haze wafers provided the opportunity to integrate the haze data as an evaluation tool in the statistical process control (SPC) methods, enabling process excursions to be flagged.

Process monitoring and qualification

Shrinking design rules and collapsing process windows are stretching metrology tool capability. For this reason
it is important that, in addition to light point defects (LPDs), the haze data in defect detection is taken into account to understand and monitor a broader spectrum of process-induced variations.

CVD and PVD processes
For CVD and PVD processes, the surface roughness and spatial frequency of metallic layers like tungsten (W) and tantalum/tantalum nitride (Ta/TaN), and the thickness uniformity and roughness for transparent layers like silicon oxynitride (SiO$_2$), low-k and photoresist (typically spin-on processes), can be evaluated using haze data. Thickness information can be extracted because the standing waves in the metallic layer cause different laser light intensities at the top layer. The haze signal can be related to other metrology data such as reflectivity, thickness and sheet resistance. The benefits of using the haze signal as a proxy for other metrology steps are that it can be combined with particle measurements, it has a very short process time that reduces overall inspection time, and a full wafer map is provided.

Tungsten CVD process
Tungsten CVD processes are evaluated in SPC tests on particles (using the SP1 unpatterned wafer inspection tool), absolute reflectivity (using the FT-700 tool), and sheet resistance (using the RS75 resistivity measurement tool). From an earlier study, the relation between reflectivity and haze was shown. This makes it possible to replace the 49-point reflectivity measurement (Figure 4), of the FT-700 and replace it with a full wafer plot from the SP1. By doing so, this measurement — using oblique incident beam and s-s-s polarization (for beam and two detectors) — can be combined with the particle measurement. An upper spec limit for haze can be determined (using the maximum reflectivity laid down by the tool manufacturer) and set for the process (Figure 5). A sequence of variations observed in the final haze value (but still in spec) of the W could be related to the use of reclaim wafers of lesser quality. The excursion was due to a variation in the process conditions: a fluctuation in temperature.

Ta/TaN Layer
The study of the Ta/TaN layers focuses more on the sensitivity of the detectors (varying sensitivities for different scattering angles) for different spatial frequencies (see the power spectral density diagram) of the wafer surface. The higher the spatial frequency, the more light will be scattered to the wide detector. The ratio of the detectors to the frequency of the wafer surfaces provides information about the overall morphology of the surface under consideration. Therefore, we could conclude that a deposition process with a higher bias provides smoother surfaces (Figure 6). AFM images confirm these findings, for the 50-50 and the 128-128 bias setting (bias$\text{TaN}$-bias$\text{Ta}$). Similarly, the copper-seed layer can be evaluated, and the self-anneal process for the different stacks can be monitored by the haze channel of the SP1. Control of this self anneal process plays a role in the suppression of defects like void formation during plating. Haze information for the barrier and copper-seed layers allows us to select the optimum material for the process, as well as to set specs for equipment SPC tests.

Oxide deposition
Oxide deposition processes can be monitored for uniformity or roughness by the haze channel. Both measurements are determined by polarizing the light in different ways. The uniformity can be evaluated by the S-polarization. The SP1 haze plot can be compared with the thickness plot of the KLA-Tencor SpectraFx thin film metrology tool (Figure 7). Any surface uniformity problem can be detected by the SP1, but not quantified. The surface roughness and also possible defect regions can be evaluated by C-polarization. The
SPC tests for particles can be extended to the measurement of haze and particles. As shown in Figure 8, the role of haze can play an important role in identifying tool defects; in this particular case, wafer cooling problems. It is interesting to note that, in all cases, haze data indicates process problems, unlike the LPD channel.

**Nano-particles**

The industry is facing new challenges concerning particle removal beyond the resolution of the state of the art light scattering tools ($\phi_{LSE} < 50$ nm). The limitations of being able to measure wafers with small particles and/or in high densities can be overcome at the full-wafer level by using haze. This method can be used to evaluate performance and uniformity for cleaning tools like megasonic cleaners (Figure 9). A lot of 30 nm particles are not removed by megasonics due to the shadowing effect of the wafer carrier. Based on the Raleigh approximation, a simple model is developed to describe the added haze of a wafer $\eta_{add}$ due to a higher density of particles $\sigma$.

$$\eta_{add} = \Omega_{tool} \cdot \Pi_{part} \cdot \sigma$$

In this equation, $\Omega_{tool}$ stands for the tool constant (influenced by laser-light-wavelength and optical characteristics) and $\Pi_{part}$ for the particle constant (influenced by parameters like diameter and refractive index). The added haze increases proportionally to the particle density.

![Figure 6. HF/LF ratio for different Ta/TaN barriers and AFM measurements. Higher bias provides a smoother surface.](image)

![Figure 7. Output file of (A) a haze measurement and (B) a thickness measurement.](image)

![Figure 8. SPC tests for 200 nm oxide using haze and the LPD channel. Cooling problems are monitored with haze in five cases, and with the LPD channel alone in four cases.](image)

![Figure 9. An evaluation of a megasonic cleaning tool for 30 nm SiO$_2$ particles. The SEM review tool is used to count particles.](image)
density. Using SEM review, a clear relationship can be then established between haze and particle density.

Cleaning performance
A spray acid tool (batch stripper) is used for chemical cleaning, stripping and etching. For the daily SPC tests, a blank silicon wafer is processed with $\text{H}_2\text{SO}_4/\text{H}_2\text{O}_2$ (10:1 ratio) for 10 minutes at 95 degrees C. In addition to detecting traditional particle defects, haze is useful for identifying other process problems. For example, when the rinse step following the acid step is not performing well, sulfuric residues will remain on the wafer surface and form ammonium sulfate crystals. The haze signal will be high because of the presence of these crystals. Figure 10 illustrates that the haze signal is too high with respect to the target value set for the Si wafers (0.05 ppm). To detect these problems and test the effectiveness of the cleaning process, the haze data is necessary, and can be simultaneously used with the LPD data.

Sealing defects
The combination of solvent adsorption and haze allows sealing defects at the surface (BEOL) to be localized and quantified. Results on different hardmasks (HM)/dielectric stacks, such as CVD HM on CVD dielectric, CVD HM on spin-on dielectric, and spin-on HM on spin-on dielectric, can be easily evaluated. Figure 11 provides an example of a CVD HM on CVD dielectrics, after CMP, treated with toluene and measured with the SP1. This haze data is analysed using the MX4.0 haze analysis capability of the SP1. The results reveal the easily-neglected condition that a clear sealing is lacking at the edge of the wafer and at certain points on the wafer surface, due to the presence of big particles.

Aknowledgements
The author would like to thank the Surfscan Division of KLA-Tencor for the fruitful and interesting cooperation in this study, and SEZ for the creation of the haze reference wafers.

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References
Simulating the Impact of Reticle Defects

A Study of Defect Measurement Techniques and Corresponding Effects on the Lithographic Process for a 193 nm EPSM Photomask

Anthony Nhiev, Jason Hickethier, DuPont Photomasks
Haiqing Zhou, Texas Instruments
Trent Hutchinson, William Howard, Mohsen Ahmadian, KLA-Tencor Corporation

Photomasks with small dense features and high mask error enhancement factor (MEEF) lithography processes require stringent reticle quality control. The ability to quickly and accurately measure reticle defects on a high-resolution inspection system and to simulate their impact on wafer printing are key components in ensuring photomask quality. Tests show that the inspection system can quickly and accurately determine sizes of most defects. The study also indicates that the simulation techniques can accurately track the lithographic results, and can be used to reduce or eliminate the use of test wafers and expensive lithography and wafer metrology time. The outcome of this study leads to better defect dispositioning by providing techniques to determine the size and printability of reticle defects.

Introduction
Photomask manufacturers typically repair masks when any visible defect is found during reticle inspection. This repair adds extra steps to the manufacturing process and increases the risk of damage to the mask. With a comprehensive analysis of defect sizing techniques, and modeling the impact to the wafer of various defect types and sizes, a better decision can be made concerning whether an individual defect will have an effect on the lithographic process. This is also beneficial to device manufacturers who periodically re-inspect photomasks between production lots and must decide when a mask needs to be replaced due to increasing number of defects. This paper will look at size measurements made by UV and DUV reticle inspection systems compared to SEM measurements on the mask. It will then model individual defects through hardware-based and software-based aerial imaging simulation to determine the impact of the defect at nominal focus/exposure. The modeling will be compared to SEM measurements on the wafer.

Test vehicle
The programmed defect mask selected for this analysis is the DuPont Photomask VT491™ Verithoro design. The mask is an embedded phase shift mask (EPSM) designed for 193 nm lithography. The photomask is fabricated with six percent transmission molybdenum silicide (MoSi) on quartz blank. The VT491 mask has a nominal design circuit of 400 nm space (reticle scale) with a 1:2 ratio pitch. The nominal contact design is 900 nm at reticle scale with a pitch of two microns. There are 20 defect types, each ranging in design size of 0 to 450 nm in 50 nm steps (reticle scale). The mask is designed to run in die-to-die inspection mode, with the programmed defect die in the middle of a seven by one die array. Figure 1 shows the defect types, design, and SEM sizes, as well as the 100 percent capture rate (shown by the darkened cells) and review measurement size found in each of two UV and one DUV inspection systems. Columns 5-9 have been omitted from this chart, as these larger defects are found by the inspection 100 percent of the time and would always be transferred to the wafer.
Photomask CDSEM analysis

Each of the 200 defects were manually measured on the mask with a KLA-Tencor 8250-XPR™ low voltage CDSEM at 1000eV. The system was calibrated using a 1000 nm pitch standard supplied with the system. The measurements were taken at the appropriate scan rotation to reflect accurate measurements of defects on corners and angled lines. High-resolution images of each defect were captured at 100,000 magnification. The defect size recorded is the maximum extent of the defect relative to the “0” column, where no defect is present. Typical repeatability of a CDSEM measurement is better than 2 nm (3 sigma).

Photomask inspection and review

Three KLA-Tencor inspection systems (two TeraStar SLF-77™ UV and one TeraScan DUV 525™ model) were used to inspect the test mask in die-to-die mode.
For each system, four inspections were conducted to complete the repeatability and sensitivity analysis. Each of the captured defects was measured using the review linewidth measurement software included with the systems. The defect sizes were graphed as a function of SEM measurements. Sensitivity analysis was performed and is shown in Figure 1. The pin-hole and pin-dot defects were detected as shown by the shading in the table. However, the linewidth, measurement review software failed to measure their size. Figures 2–4 show some of the typical defect types.

Nikon model-S305™. The standard 100 nm node DUV moat resist process was used to print the wafers. The two bare silicon wafers were first coated with DUV BARC of 0.043 µm, and then coated with DUV resist of 0.23 µm. For rows A–L, Q, and R, best exposure was determined to be 46 mJ/cm² at a focus offset of - 0.25 microns. For the contact rows M–P, S, and T, the best exposure was 38 mJ/cm² at a focus offset of - 0.25 microns. Wafers were analyzed using the KLA-Tencor 8250-XPR CDSEM at 800eV. All 200 programmed defects were measured at best focus and exposure. Measurements were performed at a scan rotation perpendicular to the defect and reflect the maximum CD change from the reference (0) column. Figure 5 displays the design defect size along with the change in CD (absolute value) using three methods: wafer SEM measurement, AIMS, and TeraSim.

**AIMS simulation and analysis**

AIMS simulation was conducted and compared for accuracy and ease-of-use with the wafer printing results. This optical lithography simulation consisted of AIMS (aerial image measurement system) Fab 193™ from Carl Zeiss, the most common system used for final qualification and dispositioning of reticle defects. It is a hardware-based simulator that requires the mask to be loaded to obtain high-resolution images that approximate the aerial image when exposed with a DUV lithographic scanner. The illumination condition was set to match the scanner’s settings. AIMS results were measured using five-pixel averaging over the reference and defect area. Intensity values were measured and recorded for both clear and dark geometry. Using the AIMS software linewidth versus threshold plot, reference regions were used to set an intensity threshold that resulted in a printed CD corresponding to the non-defective nominal space and pitch of the reticle scale. This intensity threshold was then applied to each defect region to measure CD impact on the wafer. Clear reference calibrations for image normalization was acquired approximately every hour to reduce the error attributed to laser instability.

Figures 6 and 7 show typical defects, AIMS-Fab simulation and actual mask measurements versus wafer SEM measurements. The mask values were divided by four to account for the scanner reduction. All three inspection systems match the mask SEM measurements very well. The AIMS results have a good correlation to the printed wafer results.
converted into a pair of defect and reference simulation masks used to predict the aerial image at best focus. The lithographic impact was evaluated using two methods.

First, the intensity difference metric (IDM) was calculated as described below. Consultations with various AIMS users have shown that most use a single-value intensity metric to judge the printability of reticle defects. Further, it is common to use a standard of ten percent for determining whether a defect should or should not be printed. A "**" indicates that the main feature did not print or was not predicted to print by simulation.
Figure 8a and 8b shows two examples to illustrate how the IDM is defined.

The values in the numerator are taken at the location where the test and reference aerial images differ by the largest amount. Using the absolute value ensures that the IDM is always a positive number expressed as a percent. The denominator is the normalization factor, which is calculated from the maximum range of the aerial images in the vicinity of the defect location. For the results presented here, the IDM was calculated using the prototype version of TeraSim, which can read AIMS data. The AIMS test and reference data were processed using the same software used to process the simulated aerial images from TeraSim.

\[
IDM = 100\% \times \frac{|I_{\text{Ref}} - I_{\text{Test}}|}{\text{MaxRange}} \quad (1)
\]

An example of a comparison between AIMS and TeraSim based on IDM is shown in Figure 9. The R-series defect is an over-sized clear horizontal line shown in black near the bottom of the cell. The IDM increases monotonically with defect size, as one would expect, and the match between TeraSim and AIMS is good.

A second comparison was made by matching the predicted change in critical dimension (CD) from AIMS and TeraSim to the actual wafer CD change measured on the CDSEM. The AIMS data was processed by the AIMS operator at DPI, and the TeraSim data was processed using the new prototype version. Both AIMS and TeraSim results are contour plots of simulated aerial image intensity. To extract CD values from these data, the edges must first be located by selecting a particular threshold contour. This is done by calibrating to several non-defective...
features on the wafer. This calibration step is done independently for the AIMS and TeraSim data. After this calibration, the CD difference values were calculated at each of the defective sites. The simulated CD change from TeraSim and AIMS can then be compared to each other and the wafer print results. When one makes such a comparison, caution must be exercised, because the AIMS and TeraSim data are simulations of the aerial image which do not take into account the resist processing effects. For example, previous research has shown that line end shortening (LES) is caused by multiple effects and that a portion of LES is caused by resist processing. Therefore, the amount of LES predicted by simulating an aerial image will normally be less than that seen on the wafer.

An example of this comparison is shown in Figure 10. The K-series defect is a misshapen EPSM feature shown in white on the left side of the cell. The change in CD increases monotonically with defect size, as one would expect, and the match between TeraSim, AIMS and wafer print data is good.

Conclusion
In this paper we demonstrated that the inspection station review tool is capable of predicting the size of defects within ± 50 nm for a normal line/space geometry and over/undersize contact. However, pinhole and pin dot defect types are less predictable. This study showed that both UV-based and DUV inspection systems are capable of detecting these defect types well below 200 nm, but AIMS and wafer printing correlation revealed they have no significant impact on printability. To produce highly accurate prediction beyond the inspection review tool, AIMS and TeraSim simulations can be used to estimate defects on complex design circuitry. AIMS system is well known within the industry for accuracy in simulating the lithographic process, and this data shows that the AIMS results correlate well with wafer printing. It requires the extra step of loading the mask, changing hardware settings, and capturing image for simulation. TeraSim software-based simulation achieves results comparable to AIMS system with inspection captured images as input. TeraSim is PC based software, and must use KLA-Tencor X-link™ software package to import review images. TeraSim has the advantage that its use does not require any additional handling of the reticle.

Acknowledgement
The authors would like to acknowledge Kevin Rentzsch (DuPont Photomasks, Inc.) for his assistance in setup of KLA-Tencor CD SEM file of all 200-defect on the mask; and Carl Siniard (DuPont Photomasks, Inc.) for his support in collecting AIMS data.

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References
WestWorld Attendees’ Choice Award

KLA-Tencor’s eS30 receives SST’s WestWorld Attendees’ Choice Award for Best Solution to a Problem. The electrical defects in the production process, chipmakers defect monitoring for high-volume production, which increases yields and ROI.

Best Solution To A Problem: KLA-Tencor’s e-beam inspection system combines speed and sensitivity

The eS30 e-beam inspection system provides the throughput and production worthiness required for electrical line monitoring. The eS30 combines speed, sensitivity, and ease-of-use into a single platform for all phases of the IC technology lifecycle, enabling chipmakers to reap gains in yield and fab ROI. Significant reductions in tool overhead, including wafer loading and set-up time, coupled with faster scanning speed and ease-of-use enhancements, effectively triple the throughput of the eS30 compared to the manufacturer’s eS20XP system to enable whole-wafer, high sensitivity inspection in under an hour for many applications.
PROLITH v8.0

As feature sizes continue to shrink, lithography processes are being pushed to their limits. Lithography simulation essentially must solve complex problems in both reticle and wafer manufacturing as lithographers push existing 248-nm and 193-nm technologies to smaller and smaller feature sizes through the use of increasingly complex techniques, such as off axis illumination, phase-shifted reticles, and double exposure processes. This level of sophistication demands that simulation tools be accurate, versatile, easy to use, and fast in order to support decision making across a wide range of technologies, processes, and materials.

Leading the way in this critical emerging area of lithography management is KLA-Tencor’s PROLITH software, the industry’s leading lithography simulation tool. PROLITH’s optical lithography modeling capabilities enable customers to maximize yield, more rapidly implement new processes and technologies, and increase their lithography equipment utilization.

The newest PROLITH release, version 8.0, allows lithographers to be even more efficient in resolving lithography simulation problems. With a new multi-measurement capability, lithographers can determine the best overall process settings, enabling creation of an overlapping process window that simultaneously accounts for all critical dimensions and measurements. PROLITH v8.0 enables measurement of up to 11 different locations on a cross-section and up to 22 additional, top-down dimensions with the PROLITH 3D option. These additional measurements take no additional simulation time. Additionally, metrology planes can be added or moved using a table or by drawing or dragging on a graph. Whether measuring aerial images, resist profiles, or anything in between, additional measurement information significantly helps shrink decision time. PROLITH v8.0 also includes a simulation capability for liquid immersion lithography (LIL), enabling determination of the potential performance advantages of this new process technology in meeting specific device and technology requirements.

Other new features/benefits:
- Quick viewing of full-chip GDSII or MEBES design files
- Evaluation of the impact of using a different polarization setting for each pass on the exposure tool, which helps determine which exposure process gives the best lithography process results
- Measurement of features on diagonals or on any angle, optimizing total feature performance on today’s most advanced device layouts
- Metrology data along planes that do not start or stop at a simulation grid point. New flexibility assures necessary information from the exact location desired
- Wider range of template files allows designation of default PROLITH input values so they correspond to common technology nodes, making starting point closer to actual process
- Improved PROLITH Programming Interface (PPI) documentation. PPI now includes low-level commands for working with multiple metrology planes
MetriX 100™

MetriX 100 is the industry’s first inline, non-contact metal films metrology system to provide independent measurements of film composition and thickness on product wafers. Controlling film composition and stoichiometry of new materials introduced in production of 90-nm and below devices is as important as controlling film thickness. With its versatile electron-beam technology, MetriX 100 leapfrogs current techniques, bringing a well understood and proven technology to the production floor that, for the first time, enables chipmakers to address this new challenge. This system offers advanced capabilities that meet thin film process control requirements for the 90-nm and below nodes, including SiON gate dielectric, bi-layer TaN/Ta barrier seed, and ultra-thin atomic layer deposition (ALD) barrier films.

Utilizing electron beam stimulated x-ray technology (ESX), MetriX 100’s electron beam stimulates characteristic x-rays and quantifies the x-ray intensity into composition and film thickness data. MetriX 100 also reduces the use of monitor wafers to lower manufacturing costs through small-spot measurements in the scribe line of product wafers. An easy-to-use UI enables fast, highly reliable measurements, while remote diagnostics and support capabilities ensure high in-fab productivity. Providing highly precise non-contact films measurement on product wafers, MetriX 100 incorporates the latest 300-mm advanced automation requirements, remote diagnostics, and the same user interface as the production-proven SpectraFx 100 dielectric films metrology system.

MX 4.0 (Monitor eXpert)

MX 4.0 software for KLA-Tencor’s Surfscan SP1 unpatterned wafer inspection system enables the Surfscan SP1 tool to conduct defect detection and process monitoring in a single scan — providing a fast and cost-effective alternative to many time-consuming and manual process-monitoring steps with little additional overhead. MX 4.0 enhances existing software features and introduces three new major software options that provide the SP1 with new inspection and process monitoring capabilities.

Haze normalization introduces the ability to match haze measurements between SP1 systems. Haze analysis, a powerful software analysis feature, models and detects haze defects in the SP1 haze map. Brightfield sizing enables the SP1 to provide consistent brightfield inspection results from tool to tool, taking this capability beyond engineering analysis to production worthy inspection. MX 4.0 also provides valuable new defect analysis and process monitoring capabilities for wafer and IC production that improve the SP1’s data reporting for backside inspection, haze measurements, and analysis and brightfield inspection.
Sunday, February 22, 2004

6:00 - 9:00 pm

Join us at KLA-Tencor’s 5th annual Lithography Users Forum.
Featuring technical papers on advanced solutions for CD and overlay control, photocell monitoring, simulation techniques for immersion lithography … and more.

Keynote address by:
Dr. Frank Schellenberg, Mentor Graphics
“What DFM Really Means”

Location: Techmart
Silicon Valley Room
5201 Great America Pkwy
Santa Clara, CA 95054

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