Breaking Through the Copper/Low-κ Barrier

Defect Management in Copper Devices
Part 1: From Barrier/Seed Through Post-CMP Clean

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While copper interconnects and low-κ dielectrics represent enabling technologies for current and future device performance, their use is accompanied by some unique and difficult challenges. Surface and sub-surface interconnect voids, plus copper CMP slurry and clean residues are among the most common types of defects found in the part of the copper process that begins with barrier and seed deposition, encompasses copper electroplating, annealing, and chemical mechanical polishing (CMP), and ends with post-CMP and backside cleaning. The new defect Pareto they create is founded on the unique material properties of copper and low-κ dielectrics and upon the architecture of the damascene process required to utilize these materials. These yield and reliability challenges are expected to deepen as devices evolve past the 130 nm node.

Introduction

The performance enhancements granted by copper and low-κ dielectrics come at a cost. The materials are relatively new to chip manufacturers, and their properties present some challenges, especially in the areas of interconnect yield and reliability. New defect types are arising during photolithography and etch, as well as during deposition, anneal, polish and cleaning.

Despite the difficulties, all of the world's major chip manufacturers have incorporated, or are in the process of incorporating, copper/low-κ interconnects into their devices. Microprocessors with copper are in production; copper ASICs are mostly found in pilot-lines, and copper DRAMs are in the R & D labs. In some leading technology devices, copper and low-κ have completely replaced aluminum and oxide processes at every level. Copper/low-κ technology now dominates 130 nm devices, and will be crucial to the successful introduction of 90 nm and 65 nm devices. The use of copper and low-κ materials
<table>
<thead>
<tr>
<th>Defect type</th>
<th>Process Step</th>
<th>Impact</th>
<th>Image</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voids</td>
<td>Barrier/seed deposition, ECD, anneal</td>
<td>Risk of opens in vias and trenches—device failure</td>
<td></td>
</tr>
<tr>
<td>Protrusions</td>
<td>ECD</td>
<td>Typically nuisance – CMP may eliminate</td>
<td></td>
</tr>
<tr>
<td>Copper hillocks</td>
<td>ECD, anneal</td>
<td>Nuisance</td>
<td></td>
</tr>
<tr>
<td>Remaining Metal</td>
<td>CMP</td>
<td>Interconnect shorts</td>
<td></td>
</tr>
<tr>
<td>Underpolish of Copper or barrier</td>
<td>CMP</td>
<td>Shorts</td>
<td></td>
</tr>
<tr>
<td>Overpolish</td>
<td>CMP</td>
<td>Opens or resistive leakage of copper into dielectric; thinning of stack accompanied by lower device yield</td>
<td></td>
</tr>
<tr>
<td>Scratches</td>
<td>CMP</td>
<td>Microscratches are usually considered nuisance but larger scratches may lead to opens or shorts</td>
<td></td>
</tr>
<tr>
<td>Embedded Contamination</td>
<td>CMP</td>
<td>Electrical shorts; planarity loss at the dielectric level</td>
<td></td>
</tr>
<tr>
<td>Chatter marks</td>
<td>CMP</td>
<td>May affect subsequent metallization layer; excess metal may generate shorts</td>
<td></td>
</tr>
<tr>
<td>Dielectric rip-outs</td>
<td>CMP</td>
<td>Next-level shorts</td>
<td></td>
</tr>
<tr>
<td>Peeling (adhesion)</td>
<td>CMP</td>
<td>Scratching whole wafer – device failure</td>
<td></td>
</tr>
<tr>
<td>Corrosion</td>
<td>CMP clean</td>
<td>Opens or reliability issues</td>
<td></td>
</tr>
<tr>
<td>Residual Slurry</td>
<td>CMP and CMP Clean</td>
<td>Affects subsequent metallization layer: blocked etch</td>
<td></td>
</tr>
<tr>
<td>Clean residues</td>
<td>CMP clean</td>
<td>Affects subsequent metallization layer: blocked etch</td>
<td></td>
</tr>
</tbody>
</table>

Table I. Common defect types in the copper/low-κ process.
is also predicted to lead 300 mm wafer production in the near future. Despite the complexity and scaling of this leading-edge technology, expectations are that defect densities should be the same or better than in previous-generation devices.

One of the keys to successful production of copper/low-κ devices is appropriate defect management. This paper is the first in a three-part series that will address defect monitoring from barrier/seed through cleaning, defect monitoring in the photo area, and inline electrical defect monitoring for copper/low-κ devices.

**New materials, new defect types**

Within the scope of this paper several critical process steps are considered: PVD barrier and seed deposition, copper electroplating or electrochemical deposition (ECD), annealing, CMP, post-CMP cleaning, and finally a backside clean. Common defect types associated with these processes are given in Table I.

While some of these defect types are well known from aluminum/oxide processes, many are new. **What is it about copper and/or low-κ that has introduced these defects?** Insight can be gained by examining some of the fundamental material properties of copper and low-κ insulators, and contrasting them with the better-known materials of aluminum and oxide dielectrics.

Besides its superior conductivity, copper is reputed to offer better electromigration (EM) resistance than aluminum. In reality copper offers different EM resistance from that of aluminum. Copper EM processes are dominated by surface and interfacial diffusion, while aluminum EM processes are dominated by grain-boundary diffusion. Electromigration in copper can result in diffusion of copper into neighboring dielectrics and silicon, potentially poisoning the devices by causing shorts or leaks. Thus, with copper devices, the integrity of the metal/dielectric interface is critical. It is necessary to introduce a more refractive barrier metal between the dielectric and the copper layers to encapsulate the interconnects adequately. Typically a tantalum/tantalum nitride (Ta/TaN) bilayer is used, a material that has shown excellent barrier properties up to 550 Celsius. If the barrier coverage is incomplete, or adhesion between the barrier and the dielectric is imperfect, copper may leak into the dielectric and cause performance issues, reliability issues or failure. Copper diffusion may also leave behind voids.

After the barrier layer is deposited, typically by physical vapor deposition (PVD), a copper seed layer is deposited without breaking vacuum. The seed layer is necessary to assure adequate adhesion of the copper to the barrier, with good continuity and a minimum of voids. However, the seed layer represents an additional process step compared with aluminum-based devices, and any additional step is accompanied by defects (Figure 1). If the seed layer is not continuous, the conductive path from the edge of the wafer to the center, essential for copper electroplating, is interrupted. As a result, tiny copper voids may be created during ECD. During annealing — or later, as the device ages — electromigration can drive the small voids to combine. Such voids represent the biggest yield and reliability issue in these leading-edge devices.1,3

A remedy for a discontinuous seed layer is to deposit a thicker seed layer. But with the high aspect ratio structures typically found in 130 nm devices and expected in future devices, a thicker seed layer means that the via opening could be narrowed or even pinched off from seed-layer overhang effects. A narrow opening to the via complicates copper fill, and large buried voids may result.

Voids are also introduced through the mechanism of stress migration. Film stress, induced by repeated thermal...

**Figure 1. Defect examples associated with barrier deposition or dielectric/barrier interface.**

**Figure 2. Void examples in interconnect.**
conditions affect the texture of the copper film during electroplating, which in turn affects the strength of the interface. Without adequate adhesion between copper and barrier metal, or between barrier metal and low-\(\kappa\) layers, or between copper and cap layers, CMP may tear apart the stack, causing local dielectric rip-out or delamination, or fissures at the interfaces (Figure 5). Exacerbating this problem is the low Young’s modulus of the low-\(\kappa\) materials, which causes them to flake easily.

A final and very important difference between copper/low-\(\kappa\) devices and their aluminum/oxide predecessors is that the new devices are fabricated using damascene processes, and clean steps, resulting in organic residues unfamiliar from last-generation dielectric processes (Figure 4). Residue removal — of metal, slurry or organic material — is more difficult with low-\(\kappa\) dielectrics because their surface wetting properties are more demanding, and less aggressive chemistries must be used.\(^1\)

**Adhesion** can be challenging in copper/low-\(\kappa\) devices because new materials necessitate new understanding of the physical chemistry of interacting neighboring layers. Adhesion is also a more difficult problem because the number of interfaces has been increased by the requirement for a seed layer for each copper metallization. Barrier-seed
Common practices for copper defect control

The number and variety of new defect types arising during copper processing is remarkable. Critical processing steps use new materials, processes and equipment. New processing parameters are required for ECD and anneal. The CMP consumables set is new — slurry, pad, and clean chemistry — to address new requirements for polishing copper and low-κ materials.

Defect control in such an environment requires a well-planned methodology and precisely the right set of inspection tools. Because copper/low-κ is a relatively immature process, single-wafer excursions dominate. Furthermore, the ratio of nuisance defects to yield-limiting defects is high. In this realm of defect management, extensive sampling is necessary for adequate excursion monitoring. Also, tracking defects by type is critical to yield learning and tool monitoring in the presence of high nuisance counts.

While double-darkfield inspection is generally preferred for film levels, such as interlayer dielectric and copper ECD, a study of several of the most successful foundries and integrated device manufacturer fabs in the US, Asia and Europe, has shown that the most common tool set for successful defect control at copper CMP is a mix of high resolution imaging and double-darkfield inspection. During the development and ramp phases, high-resolution imaging is used for a greater percentage of inspections. As yield learning progresses and wafer sampling demands increase, double-darkfield inspection is increasingly used to meet the requirement for higher throughput (Table II).8

Post copper CMP, generally two wafers per lot are inspected in both logic and memory areas to measure CMP and ECD defectivity. At the same time, the substantial wafer-to-wafer variation from under-polish and residue defects drives the need for high within-lot wafer sampling. Here,
double darkfield inspection is often chosen for its high throughput capabilities (Table III).\(^8\) Inline electrical testing using voltage-contrast mode on an e-beam inspection system is essential for detecting buried voids — perhaps the most critical defect type generated within the copper process. This key technology will be explored in a later article in this series. The use of automated macro inspection, replacing manual inspection in the detection of gross polish defects, will also be explored in a later article, as will the use of unpatterned wafer inspection for tool qualification within the copper module.

**Case studies**

Short-loop experiments of various kinds take place during the copper process, to work toward resolving defect problems unique to copper/low-\(\kappa\) devices. Once the common defect types have been identified and sourced, mostly by the yield engineers, defect management typically becomes the responsibility of the process engineers. The process engineers take ownership of statistical process control (SPC) charts and control limits, and manage the defect excursions within their module. By taking over the tool monitoring, the process engineers free the yield engineers to focus on process and inline monitoring.

Effective tool monitoring during the copper process necessitates closely monitoring each deposition, polishing and cleaning system. The inspection system needs to be situated close to the process tools, not only for convenience and to reduce response time to excursions, but also to minimize exposure time for the copper layers before capping. Finally, contamination considerations often dictate that the inspection system be dedicated to the copper area.

**Texas Instruments** in Dallas, Texas, described the detection of surface and sub-surface voids using optical and e-beam voltage contrast inspection, respectively, in a recent article. TI’s Kilby Development Center (KFAB) used double-darkfield inspection to

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**Table II.** Summary of technologies used by eight fabs to control defects in the copper process. These fabs are at various points between yield ramp and production. Adapted from Reference 8.

<table>
<thead>
<tr>
<th>Inspection Technology</th>
<th>4 Foundry and 4 Logic Fabs, 130 nm</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>e-beam High Resolution Imaging Double-Darkfield Recommended Technology</td>
</tr>
<tr>
<td>Barrier/Seed</td>
<td>0 1 4 Double-darkfield</td>
</tr>
<tr>
<td>Copper ECD</td>
<td>0 1 1 Double-darkfield</td>
</tr>
<tr>
<td>Copper CMP, M1-M2</td>
<td>3 7 3 High resolution imaging/e-beam</td>
</tr>
<tr>
<td>Copper CMP, M3+</td>
<td>3 5 5 High resolution imaging/Double-darkfield/e-beam</td>
</tr>
</tbody>
</table>

**Table III.** Summary of typical sampling plan recommended to control defects in the copper process during ramp and production. Adapted from Reference 8.

<table>
<thead>
<tr>
<th>Recommended Technology</th>
<th>Typical Sample Plan</th>
<th>% Lots</th>
<th># Wafers/Lot</th>
<th>% Wafer Area</th>
</tr>
</thead>
<tbody>
<tr>
<td>Barrier/Seed</td>
<td>Double-Darkfield</td>
<td>25-50</td>
<td>3-5</td>
<td>100</td>
</tr>
<tr>
<td>Copper ECD</td>
<td>Double-Darkfield</td>
<td>50</td>
<td>3-5</td>
<td>100</td>
</tr>
<tr>
<td>Copper CMP, M1-M2</td>
<td>High Resolution Imaging</td>
<td>25-50</td>
<td>2</td>
<td>100</td>
</tr>
<tr>
<td>Copper CMP, M3+</td>
<td>Double-Darkfield</td>
<td>100</td>
<td>5-15</td>
<td>100</td>
</tr>
</tbody>
</table>

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**Figure 8.** KLA-Tencor’s AIT darkfield inspection was implemented post-ECD and post-CMP, and utilized to partition the source of patterning and underlying defects.
uncover a characteristic spatial pattern of surface voids in the defect wafer maps after ECD, after CMP, and after the CMP clean, for a 130-nm copper dual-damascene device. This study revealed that the root cause of the voids was in the ECD; the voids were subsequently enlarged and uncovered by CMP and the post-CMP clean (Figure 8). TI developed an out-of-control protocol, and transferred the process to production.3

A second experiment by the same group used an inline e-beam inspection system in voltage contrast mode to detect sub-surface voids that were causing yield problems. Screening the pre-ECD seed conditioning, the pre-ECD rinse conditioning, and the post-ECD anneal, they discovered that the anneal was the problematic area (Figure 9). By changing the anneal conditions they reduced the sub-surface void formation to acceptable levels.3

Infineon Technologies in Dresden, Germany, used double-darkfield inspection to systematically investigate the effectiveness of various post oxide CMP cleaning process parameters on memory products, and their potential impact on final device yield (Figure 10). As the post-CMP rinse procedure was varied, electrical characterization showed post-CMP defects primarily affected the wafer’s subsequent metallization layer. Slurry agglomeration defects had the greatest impact on yield, causing shorts between metal lines. Because nuisance defects showed the greatest variation in number as the rinse parameters were varied, tracking by total defect count would not have been useful. Instead, tracking by defect type was critical, and the inspector’s Real Time Classification option (RTC) was able to distinguish “killer” slurry agglomeration defects from nuisance defects (flat, chopstick-shaped silicon oxide, and micro-scratches) with no impact on throughput (Figure 11). Infineon determined the optimum cleaning rinse solution and process time — and the result proved to be a compromise between maximizing device yield and minimizing both the process time and cost of consumables.6

TI DMOS 6, TI’s first 300 mm fab, was interested in ramping their 130 nm copper devices on 300 mm wafers quickly. They faced some challenges, particularly because they were bringing up new tools (Figure 12). In phase I (process qualification and integration) they used the KLA-Tencor 2350, high resolution imaging inspector to determine that more than 30% of the die on the wafer were affected by copper seam defects, post CMP. The defect provided problems for vias landing on the leads, and for line resistivity (Figure 13). DMOS6 was able to optimize their CMP process and eliminate the galvanic corrosion that was responsible for the copper seam defects.

In phase II (yield ramp) a missing-metal defect, detected post CMP by high resolution imaging, was affecting 3-5% of the die, with excursions affecting up to 20%. The source was found to be TaN barrier particles interfering with the subsequent copper plating. After improvements to
the barrier metal process, the TaN particles were brought under control.

High resolution imaging was also the technology of choice for copper CMP monitoring during phase III (yield entitlement). A new defect signature was detected on a set of wafer maps, and was traced to particles coming from degraded CMP brushes. After the brush was replaced, the defect source was eliminated.

During each of these phases, e-beam inspection with the KLA-Tencor eS20XP was used to complement the high resolution imaging, with success at each phase. TI DMOS 6 plans to use a similar high resolution imaging and e-beam inspection strategy to bring up their 100 nm process.

AMD Fab 30, described an effective tool monitoring strategy for their copper CMP module, in which both single-wafer excursions and high nuisance rates — especially in the form of microscratches — were present. They used KLA-Tencor’s AIT, a high throughput, double-darkfield inspection system equipped with RTC and High Resolution Defect Classification (HRDC) to monitor all copper layers for their most critical defect types: residual copper, copper precipitates, copper corrosion and slurry residue, and separate these from defect types of less importance: microscratches, previous-layer defects, particles and pattern defects. RTC was able to accomplish this discrimination with no discernible impact on throughput. A new feature called “trigger sampling” directed samples of defect images from wafers flagged by RTC, to undergo HRDC. HRDC examined a number of defects on the wafer to identify defects of interest (Figure 14). Whenever the population of any of these defect types exceeded its (layer-dependent) threshold, HRDC declared the tool out of control, and appropriate corrective measures were taken.

AMD feels this is a practical solution for their “high volume high inspection sample production facility.” They reported a cycle time improvement of 30% within the copper CMP module, a reduction in false excursions, faster time to results, and a higher capture rate of critical defect types. With this new methodology, AMD Fab 30 has been running in production since November 2001, and considers the methodology part of their process of record.

TI KEAB was using the AIT double-darkfield inspection system to monitor full lots of a 130 nm copper single-damascene test-chip device, post CMP, when they discovered an excursion. Further analysis showed that most defects were coming from slot 24, the first wafer going into the CMP polisher, and they were able to address the problem (Figure 15). In this case, it was essential that they were monitoring the whole lot, or they would have had much more difficulty uncovering this first-wafer effect.

TI's general tool monitoring strategy is to dedicate the AIT double-darkfield inspection system to the copper CMP area in the copper “wet room,” and set up simple, speedy (40 wph) scans after via and trench CMP. They use recipes optimized for CMP surface...
defects, which together with RTC, minimize the effects of nuisance counts. They inspect full lots, correlate in-line defects to electrical data, reduce outliers, and work to understand the process variation. The main defect type at via CMP has been slurry residue, while CMP scratches have dominated at trench CMP. When excursions are understood and brought into control, TI reduces the sampling rate. This methodology has driven a dramatic yield improvement at trench, and a more modest improvement at via. The methodology has also been implemented in TI’s 300 mm fab. 7

TI demonstrated the value of utilizing the 23xx high resolution imaging inspector as a reference system, ensuring the capture of all defect types of interest for that module, then using the resulting Pareto chart and defect map to set up appropriate recipes on the higher throughput, double-darkfield system. 1, 7 They found that the double-darkfield system was able to capture all CMP defect types that the high resolution imaging system could capture. They also found that the high-resolution imaging technology was especially sensitive and uniquely effective in capturing ECD and integration defects (seam/edge voids, pattern defects, etc.).

While specific methodologies and tool sets throughout the copper process are determined by many factors, such as product type, layer, and dominant defect species, a few general observations can be made. Extensive sampling is recommended for adequate monitoring of single-wafer excursions. Tracking defects by type is critical for yield learning and tool monitoring in the presence of high nuisance counts. Finally, utilizing a mix of high-resolution imaging and double-darkfield inspection, migrating to predominantly double-darkfield inspection as wafer sampling demands increase (requiring higher throughput inspection) has been a successful tool utilization strategy in many fabs.

What’s ahead?

Copper and low-κ dielectrics are enabling technologies for future product scaling. Yet, as critical dimensions are pushed down to 100 nm and beyond, some of the current challenges in electromigration and reliability are likely to become increasingly difficult. And new issues will arise. Karen Maex, strategic research coordinator for interconnect technologies at IMEC, recently discussed concerns about the specific resistivity, porosity of the low-κ dielectrics, and the lack of an effective test for electromigration. 2

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**Figure 14.** SPC charts to catch defects of interest with IMPACT High Resolution Defect Classification.

**Figure 15.** CMP trench defect per slot.
The effective resistivity specification of the International Technology Roadmap for Semiconductors for 90 nm to 32 nm may not be possible to meet, primarily because specific resistivity rises as line widths shrink. At linewidths of 100 nm the specific resistivity is twice that of a 200 nm line, and at 60 nm the specific resistivity triples. This effect may be related to the fact that the line widths are becoming comparable to the length of the mean free path of electrons in copper, promoting inelastic scattering at the copper-barrier sidewalls.2

Some companies are currently experimenting with mesoporous materials as low-κ dielectrics. These materials contain interconnected pores 2 nm in diameter or greater, a means of achieving even lower κ values. The problem with high porosity materials is that they are vulnerable to penetration by any stray molecules of gas or vapor. Such contamination would raise the effective κ value, and diminish the value of the presumed low-κ dielectric. To mitigate this potential problem, the seal between the dielectric and the barrier metal layer would have to be nearly perfect.2 Chemical vapor deposition (CVD) of the barrier-seed layer should be more successful than PVD for coating the irregular sidewalls presented by the porous low-κ dielectric — but CVD of Ta/TaN has its own set of problems such as contamination. The more likely candidate for managing deposition on the porous sidewalls is a relatively new technique called atomic layer deposition (ALD).10 However, perhaps a more serious problem than coverage of irregular sidewalls is having residual polymer left in the pores after etch — this may be a difficult integration problem.11

Another probable upcoming challenge as the industry reaches the
90 nm and 65 nm nodes is copper fill. With a barrier/seed layer of 1100 Å (field thickness), thick enough to ensure adequate continuity on the via sidewalls, the opening to a 65 nm via would be shrunk to 150 Å, making copper fill very challenging.11 Voids will likely continue to be a dominant defect mechanism as design rules shrink and high-aspect ratios remain.

Finally, a new method for testing for electromigration will likely be necessary. Currently these tests require high temperatures, which can cause film stress, especially in low-κ materials. Furthermore, grain growth can occur during a high temperature test, and subsequent relaxation of film stress may be accomplished by void formation.12 Without an effective test for electromigration, the reliability of the low-κ device will be uncertain.2

In the face of these challenges, accurate and timely defect detection becomes even more critical. As the industry moves forward, with solutions driven by new materials, new architecture and new processes, defect inspection must stay one step ahead. Shorter-wavelength light sources, reaching into the UV, will enable greater sensitivity (see sidebars). At the same time, new algorithms in data processing and data management will prove critical to success. Hardware and software improvements must work to keep throughput high and manage costs.

**Summary**

Copper interconnects and low-κ dielectrics are enabling technologies for device performance; at the same time they are accompanied by some new and difficult challenges. These challenges may deepen as devices evolve past the 130 nm node. Surface and sub-surface voids, slurry and clean residues are among the
most common kinds of defects found in the parts of the copper process that begin with barrier/seed and end with cleaning. The new defect Pareto they create is founded on the material properties of copper and low-κ dielectrics. The architecture of the damascene process also contributes strongly in determining the defect Pareto charts for the new devices.

Several successful fabs have shown that defect control in the copper process can be optimized by: (1) dense sampling to quickly manage single-wafer excursions, (2) tracking by defect type to mitigate the influence of nuisance defects such as microscratches, and (3) selecting a mix of inspection systems that enables capture of all relevant defect types while maintaining adequate throughput to meet cost of ownership targets.

Acknowledgements

The authors would like to thank Arun Chatterjee for critical reading of this manuscript.

References

8. Raleigh Estrada, “Common Practices in Defect Control within the Copper Module.”
There used to be a time when high-yield copper interconnects only existed in your imagination. But now, they can be a reality. KLA-Tencor has the tools and strategies to help you find, analyze, and fix the defects that most greatly impact device yield – such as via voiding, opens and shorts, and copper CMP corrosion. But that’s only part of the story. We also enable you to accurately and reliably measure film uniformity, giving you what you need for inline parametric control of copper/low-k film stacks. The result? A copper interconnect yield so high, you’ll want to shout it to the world.

For solutions and strategies to accelerate copper yield, visit our Cu Xpress website at www.kla-tencor.com/CuXpress

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