Managing Within Budget
Overlay Metrology Accuracy in a 0.18 µm Copper Dual Damascene Process

Bernd Schulz and Rolf Seltmann, AMD Saxony Manufacturing GmbH, Harry J. Levinson, Technology Research Group, AMD, Joel Seligson, Pavel Izikson and Anat Ronen, KLA-Tencor Corporation

As overlay budgets shrink with design rules, the importance of overlay metrology accuracy increases. We have investigated the overlay accuracy of a 0.18 µm design rule copper dual damascene process by comparing the overlay metrology results at the after develop (DI) and after etch (FI) stages. The comparisons were done on five process layers on production wafers, while ensuring that the DI and FI measurements were always done on the same wafer. In addition, we measured the in-die overlay on one of the process layers (poly gate) using a CD SEM, and compared the results to the optical overlay metrology in the scribe-line. We found that a serious limitation to in-die overlay calibration was the lack of suitable structures measurable by CD SEM. We will present quantitative results from our comparisons, as well as a recommendation for incorporating CD SEM-measurable structures in the chip area in future reticle designs.

Introduction

It is common practice to measure overlay using dedicated scribe line targets at the after develop (DI) stage in lithography. Applying this method one assumes that the overlay measurements from the scribe line targets are a good representation of the true overlay in the device area. The obvious discrepancy between the large box-in-box or bar-in-bar structures in the scribe line and the much smaller device structures may lead to questioning if this assumption is still true in an actual production process. It was shown in earlier studies[1,5] that this overlay metrology method has the potential to introduce unwanted errors in a production process, which are difficult to detect at the overlay measurement step itself.

AMD Fab 30 in Dresden, Germany, produces logic integrated circuits using a copper dual damascene technology with—at the time of this work—0.18 µm design rule. Although the process was well in control in terms of overlay, there was a need to arrive at a

reasonable understanding of any systematic overlay problems and "hidden errors,"[1] especially towards the next design rule shrink to 0.13 µm. In the case of advanced process control applications for overlay, for example, accurate overlay measurements will be a stringent requirement. The efficiency of those applications depends significantly on the quality of the overlay data that are used.

Accuracy studies normally require calibrated artifacts or independent reference measurements. Until now, calibrated overlay standards have not been available. But even if they were available, one could determine only the degree of agreement between the standard and the tool reading. The question as to whether the overlay measurements from scribe line targets are a good representation of the overlay in the device area would still remain open. Other independent measurement methods, which are able to gather overlay information on real device structures, are needed to answer this question. A major disadvantage of almost all suitable reference methods (for example, an AFM) is their very low throughput compared to optical measurements. For our studies we used an automated CD SEM to make reference overlay measurements in a reasonable time.

The various contributors to overlay accuracy (or loss of accuracy) are schematically represented in the pie-chart of Figure 1. Contributors such as TIS (tool induced shift), TIS-3σ (variation of TIS across the wafer), tool-to-tool matching and measurement precision (repeatability) originate in the overlay metrology tool. The wafer features, the stepper, and the process determine the two remaining contributors:

1. DI/FI bias, denoted by "DI-FI," is the difference between the DI-overlay and FI-overlay.*

2. The difference between the overlay as measured on the overlay targets in the scribe-line and as measured on device structures inside the die area, denoted by "In-die."

The DI/FI bias is a well-known problem in the back-end of aluminum technology.[2-4] We would expect it to be smaller for copper dual damascene, due to the completely different metal deposition and definition process. However, we wanted to characterize it in order to understand its contribution to the overlay accuracy budget. The difference between scribe-line overlay and in-die or in-die overlay is also well known.[5] This is a problem whose significance is on the rise with shrinking design rules.

In this paper we have measured the DI/FI bias for five process layers from the 0.18 µm design rule copper dual damascene process. The scribe-line-to-in-die difference was measured on only one of the layers, due to the difficulty of finding suitable metrology features. We have combined these results with the overlay tool performance to arrive at a comprehensive view of the components of overlay accuracy for 0.18 µm copper dual damascene technology. We have also identified the need to incorporate CD SEM measurable structures in future reticle designs.

Optical overlay metrology

The goal of the optical overlay metrology in this project was to establish the tool-dependent accuracy contributors, as well as to quantify the DI-FI difference. The optical FI-overlay data were also used as the comparison data for the scribe-line-to-in-die metrology. Most of the optical overlay metrology was performed on KLA-Tencor's 5200XP overlay metrology tools in
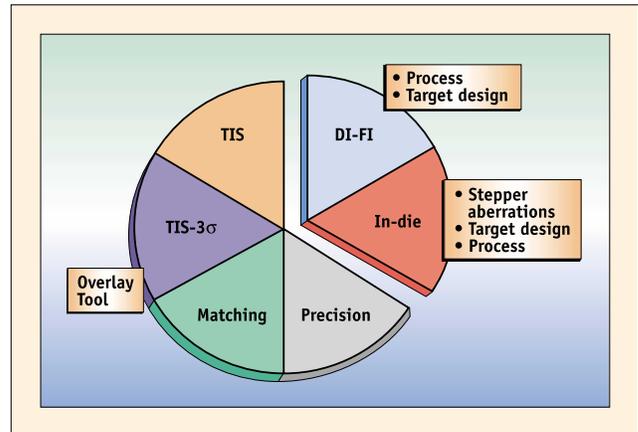

Figure 1. Overlay measurement accuracy contributors. Relative magnitudes can vary from those indicated in this figure, as will be seen later in this paper.

AMD Fab30. In order to see a cross-generational tool-to-tool comparison, additional measurements were performed on a new Archer 10 overlay metrology tool at the KLA-Tencor site.

Taking into account the complexity of the manufacturing process, only five representative production layers—poly gate, local interconnect, contact, via 2 and metal 3—were selected for this investigation. Each of these layers includes an etch operation. They represent different stages of the manufacturing cycle (front end, middle, and back end of the line) and show differences in the overlay target design.

The overlay recipes were generated using standard procedures. An identical pattern of nine measurement fields and five targets within a field was defined in the recipes for the after develop stage (DI) and the after etch stage (FI). The performance of all recipes was verified to be well within specifications for precision, TIS, and TIS-3σ. For the specific goals of this paper, we performed the following non-standard measurements on each layer:

• We collected through-focus overlay data in order to establish the effect of the metrology tool focal setting on the overlay values.

• We characterized TIS separately for each measurement site in order to evaluate the effect of average-TIS calibration versus TIS-per-site calibration.

---

* DI (Develop Inspect) measurement after developing the resist.
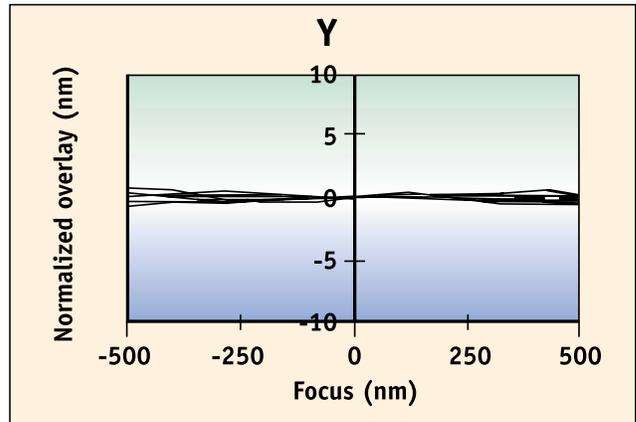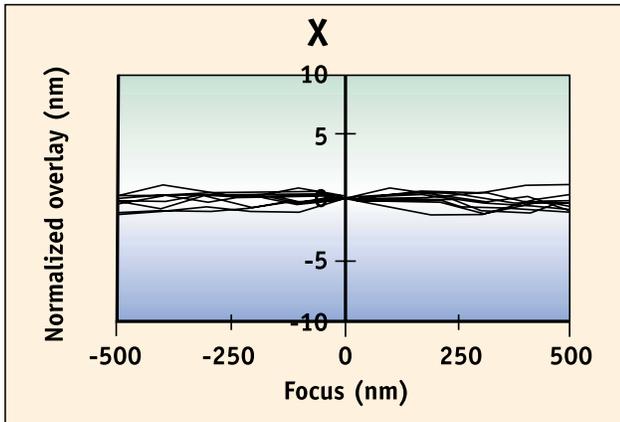 FI (Final Inspect) Measurement after the etch.

Figure 2. Poly gate FI overlay using single focus. The overlay of each site has been normalized to zero at zero focus.

Establishing FI reference

For optical overlay measurements, one of the significant overlay accuracy contributors is the difference between DI and FI measurements. At the DI stage the box (or bars) from the previous (alignment reference) layer is often covered by a film (stack), which will be structured in the following etch step. Possible asymmetries in step coverage, interference or other effects lead then to false or noisy DI overlay measurements. Since the overlay targets at the FI stage are clear, well defined, and of good contrast, we will consider the FI overlay as a reliable reference.

To validate the quality of this reference, we measured the FI overlay using different metrology modes of the 5200XP and characterized the effect of the measurement focus on the overlay results. In Figure 2 we show the normalized overlay for the poly gate layer, as measured by the single focus method ("single grab" of the

5200XP). We have normalized the overlay of each site to zero at zero focus, in order to expand the scale and be more sensitive to any deviations as a function of focus.

Each line corresponds to one of the nine measurement sites on the wafer, and the results are given through a focal range of ±500 nm. One can observe that, for each site, the overlay is independent of the measurement focus to within 1-2 nm. In Figure 3 we show the difference between the poly gate FI overlay values as measured using two methods: single focus and double focus ("double grab" of the 5200XP). The difference between the two modes is within ±2 nm around the zero focus, with slightly higher values further from zero focus. Since there is no obvious conflict between the measurements at single focus and double focus, we feel comfortable taking the single focus FI overlay at zero focus as the FI reference figure. Similar results were obtained for the other layers.
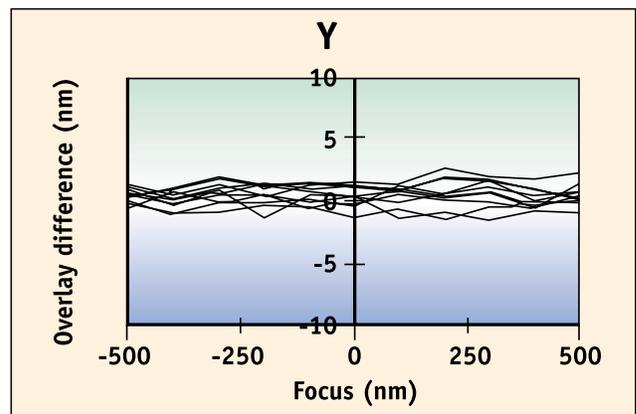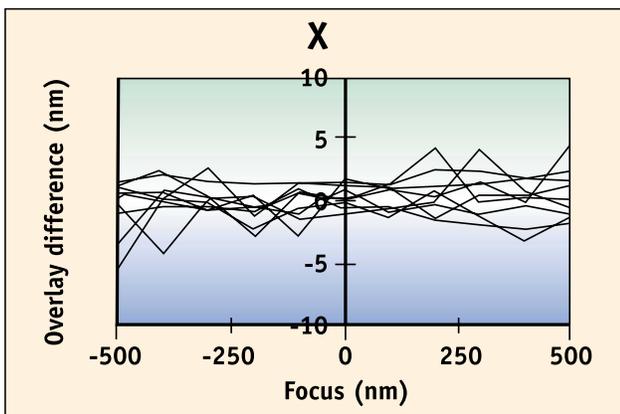

Figure 3. Poly gate FI overlay comparison using single focus and double focus. Overlay difference = (single focus overlay) − (double focus overlay).

DI/FI Bias

The DI/FI bias was measured in the following way:
- At the DI stage, a wafer was identified by its serial number and lot number.
- Overlay was measured using the standard sampling plan and recipe.
- The lot continued to the etch process.
- Once the lot returned from etch, the same wafer as in the DI stage was identified.
- The FI overlay was measured on the same locations as in the DI stage.

The results for worst case DI/FI bias are shown in Table 1 for the five process layers. We have shown the results for both average-TIS calibration (using the wafer average of TIS for calibrating all sites), and for site-by-site TIS calibration. One can see that 2-3 nm may be gained with site-by-site TIS calibration.

	DI-FI (nm)	
	Average TIS calibration	Site-by-site TIS calibration
Poly gate	10	7
Local Interconnector	5	3
Contact	10	8
Metal 3	5	5
Via 2	10	N/A

Table 1. DI/FI Bias.

DI/FI bias and its effect on modeled overlay

Another view of the effects of DI/FI bias is offered by using stepper analysis: we have calculated the stepper corrections for two of the layers (poly gate and local interconnect) for both the DI and FI case. In order to simplify the comparison, we reported the maximum DI and FI overlay differences, as predicted by the overlay model appropriate for scanners,[6] for both interfield and intrafield cases. The maximum values were calculated at the wafer edge (interfield) and field edge (intrafield). For the analysis, we used KLA-Tencor's KLASS 4 overlay metrology analysis application. The flow of the calculations was as follows:

1. Analyze the DI overlay data to produce the stepper corrections.

2. Calculate maximum predicted overlay errors—interfield and intrafield —based on modeled errors only.

3. Repeat steps 1-2 using the FI data.

4. Calculate the differences between the results from steps 2 and 3.

The maximum DI/FI differences are shown in Table 2.

Difference in nm	Interfield	Intrafield
Poly gate	10.2	2.7
Local Interconnect	2.3	1.7

Table 2. Maximum DI-FI differences as predicted by stepper model.

DI/FI Bias across the wafer

It is instructive to present some of our results as vector maps on the wafer. In Figure 4 we compare the DI/FI bias of poly gate and contact layers. Although, in both cases the maximum DI/FI bias is around 10 nm, the behavior is different: In the case of the poly gate layer, the DI/FI bias is random across the wafer, whereas for contact it shows a spiral behavior, indicating a process (possibly CMP) induced effect on the DI/FI bias.
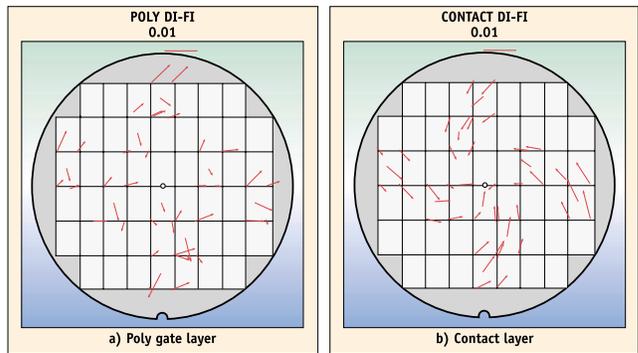

Figure 4. Vector map of the DI/FI bias—poly and contact layers.

Tool-to-tool matching

As tool-to-tool matching is one of the accuracy contributors, we measured a subset of the layers on a new Archer 10 at the KLA-Tencor site. The worst-case values (minimum and maximum) are shown in Figure 5 below. In most cases, the worst-case matching across two
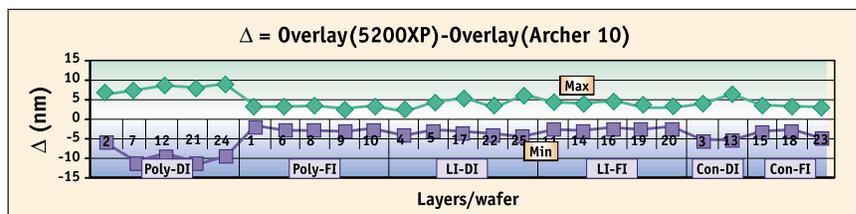

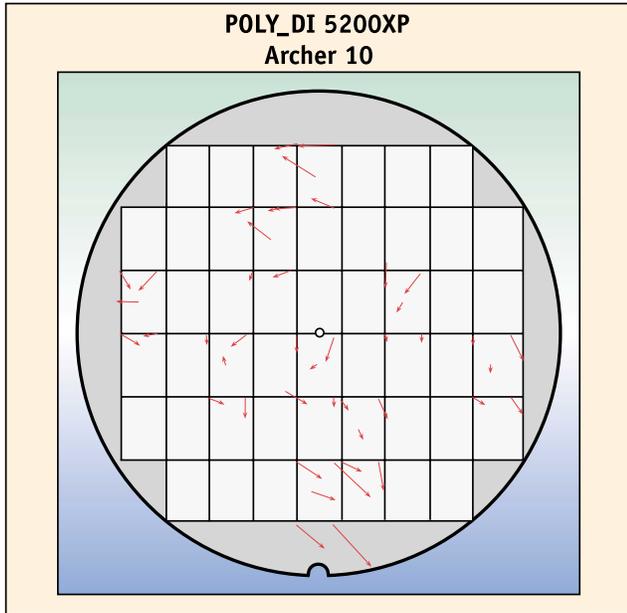Figure 5. Tool-to-tool overlay comparison.

Figure 6. Vector map of poly-DI tool-to-tool differences.

Figure 7. Overlay definition for x-direction (same definition is valid for y-direction).

tool-generations was around 5 nm. Only the poly-DI layer exhibits a worst-case around 10 nm. As can be seen from the vector map representation of the tool-to-tool differences (Figure 6), a local maximum in field (0,-2) is responsible for the somewhat elevated tool-to-tool difference. Further investigation revealed that this was due to a significant process-induced variation in the overlay targets.

Overlay measurement with CD SEM

For our overlay accuracy study it was important to find a suitable independent reference measurement method. Considering the automation capabilities and the high throughput of a CD SEM, it was adapted for overlay measurements (in our case a KLA-Tencor 8100XP CD SEM was used). Compared to an optical overlay metrology tool, a CD SEM can achieve significantly higher magnification, and direct overlay measurements on in-die structures can be carried out. Nevertheless, there are also a couple of limitations which have to be taken into account.

Optically transparent films are usually opaque for an e-beam. This means that structures from previous layers (reference boxes) covered by a film (stack) are invisible in the CD SEM image, and so DI-overlay measurements are impossible. Not so for FI-overlay measurements; if the structures of interest show edges from the actual and the previous layer in the CD SEM image, overlay
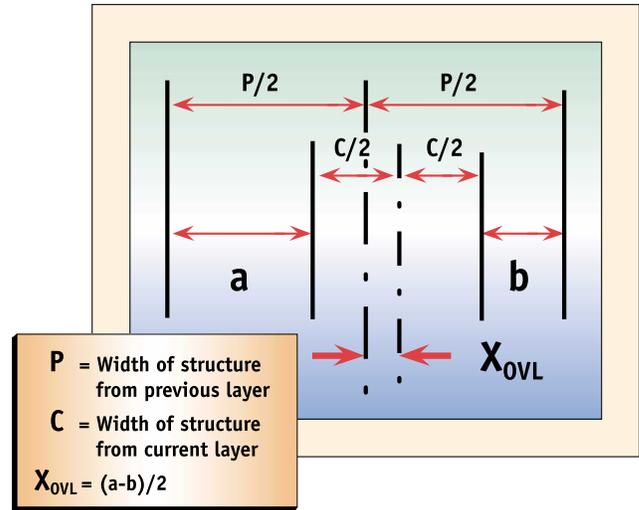
information can be obtained measuring the distances a and b (Figure 7).

In order to use this fairly straightforward technique as a reference, one should consider and possibly quantify the following potential error sources, which could affect the correctness of the overlay results:

1. Interaction of the e-beam with the sample, such as charging or carbon contamination.
2. Non-orthogonality between the x- and y-scan directions.
3. Difference between the x- and y-magnifications (aspect ratio).
4. Beam alignment.

Interaction of the e-beam with the sample can be minimized when both distances a and b are derived from the same scan signal. All edges of interest therefore will be equally charged or contaminated. Non-orthogonality between the x- and y-scan direction and the difference between the x- and y-magnifications are important CD SEM tool parameters, which are monitored and maintained within very tight tolerances for normal CD SEM operation. Beam alignment was checked carefully in every case before overlay measurements were started.

Only one question remains to be answered: is TIS also a systematical error for CD SEM overlay measurements which needs to be taken into account? In order to answer this question, TIS measurements were performed on in-die structures for the poly gate layer. As we expected,

Target 1		Target 2		Target 3		Target 4		Target 5		Average T1-T5(nm)	
TIS X	TIS Y	TIS X	TIS Y	TIS X	TIS Y	TIS X	TIS Y	TIS X	TIS Y	TIS X	TIS Y
-1.34	0.33	-1.38	0.52	-0.64	1.19	-0.81	0.27	-0.69	0.05	-0.98	0.47

Table 3. TIS (in nm) from five in-die structures at poly gate layer averaged over nine fields.

TIS for CD SEM overlay was found to be very small (Table 3). Therefore, there was no need to correct the CD SEM overlay results for TIS in any of our experiments.

As the next step for validating the CD SEM overlay measurement as a reference, we measured the standard overlay targets in the scribe line, both with the optical overlay tool and with the CD SEM. Although such large structures are not well suited for the CD SEM, a good correlation between optical FI-overlay and CD SEM measurements was established for the poly gate (Figure 8). Note that for this experiment a wafer rotational overlay error was introduced on purpose in the scanner job in order to increase the overlay range. One can interpret our results as an additional legitimization for the earlier made assumption to take the optical FI-overlay as a reference.
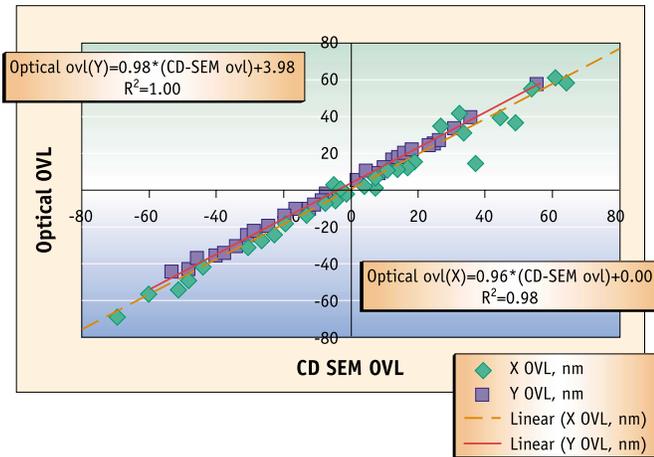

Figure 8. Correlation between optically and CD SEM measured overlay from scribe line targets at poly gate (all units in nm).

Now it was logical to proceed with the in-die overlay measurements. To our surprise, it was very hard to find appropriate structures, within the layout of the die, which would meet the following requirements:

1. The structures are symmetrical with straight and parallel edges, visible to the CD SEM, with edges from both the current and previous layer, and edges in both x- and y- directions (See Figure 7).

2. The same structures can be found close enough (within 1 mm) to the location of the scribe line overlay targets.
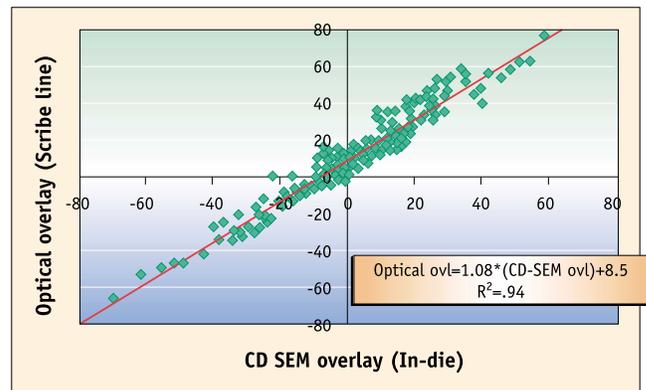

Figure 9. Optical overlay (in scribe-line) versus poly gate overlay measured with CD SEM (Both in nm).

As a consequence of the lack of such structures in other layers, in-die overlay measurements could be performed only for the poly gate layer. We chose poly gate structures, which were located in close proximity to the standard optical overlay targets in the scribe line. The results from the optical overlay measurements in the scribe line against the CD SEM measurements of the poly gate overlay are shown in Figure 9. These data are again from the wafer with introduced rotational error as in Figure 8.

One can observe a fairly good fit, with a slope close to unity and intercept <10 nm. Maximum deviations from the best linear fit are 15 to 20 nm. Our first impulse was to attribute these deviations to the small, but non-zero, distance between the optical overlay targets and the poly gates. Consequently, we expected to

reduce these deviations by calculating the intrafield scanner model parameters from the optical overlay measurements, and by using the model to predict the overlay at the poly gate locations. These predictions, however, made the situation somewhat worse.

We had already shown above (Figure 8) that there is good agreement between optical and CD SEM measurements on the same structure. Reticle errors could be another potential source for scribe-line-to-in-die errors, with the third being pattern placement error, due to the different lithographic placement of the different feature sizes of the overlay target and the device itself. For a quantitative analysis, we modeled the intrafield overlay field by two models: one based on the optical overlay measurements, and the other based on the CD SEM measurements of the poly gate overlay. We then calculated the difference field between the two results, with a graphical representation in Figure 10. The maximum difference turned out to be 18 nm, and we took this to represent the overlay difference caused by the combined pattern placement error between the two structures and, consequently, the scribe-line-to-in-die error. Contributions to differences between optical overlay measurements and in-die measurements due to the lens must be constant along the scan. Accordingly, there are some differences caused by other factors such as the reticle or CMP, but these have not been clearly identified.

Accuracy summary

Our results for the accuracy contributors are summarized in Table 4. For the poly gate, we have also presented the results graphically in Figure 11. One can see that the largest contributor is the scribe-line-to-in-die difference, followed by tool-to-tool matching and DI/FI bias. The other, tool-related, contributors are smaller.
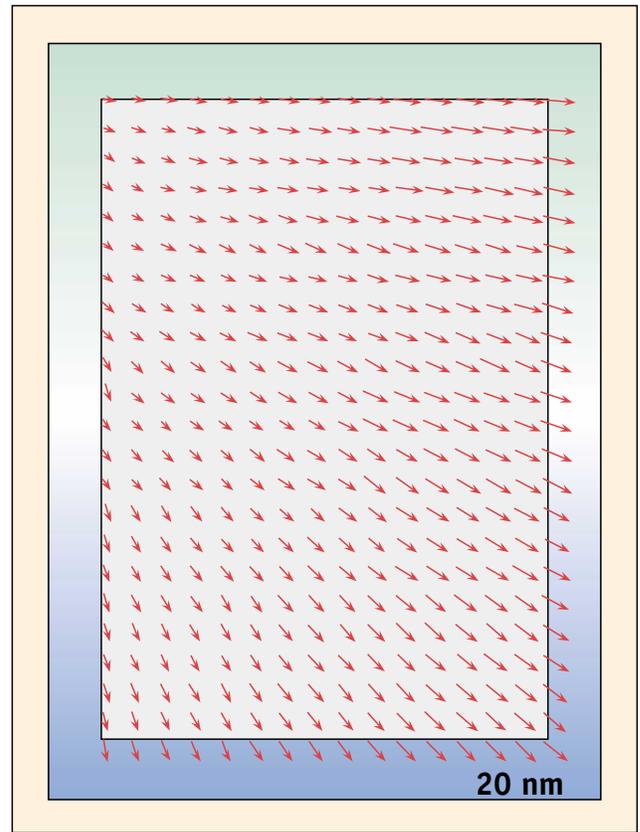

Figure 10. Difference between the two modeled intrafield overlay fields (optical versus CD SEM).

Conclusions

Overlay accuracy was investigated and quantified for a 0.18 μm design rule copper dual damascene production process. The levels of contribution from the individual sources of inaccuracy to the total inaccuracy were estimated.

A methodology to measure overlay on in-die structures was tested. In order to take full advantage from CD SEM overlay measurements special, standardized in-die overlay metrology structures should be implemented into logic device layouts. It might be also beneficial to add specific CD SEM overlay functionality (automated routines and output formats) into future CD SEM software releases.

All the major contributors to loss of accuracy (scribe-line-to-in-die differences, DI/FI bias, tool-to-tool matching) are well within 20 nm. Especially, the differences between the

Differences in nm	DI-FI		Tool-to-tool	Scribe-line to In-die
	Average TIS calibration	Site-by-site TIS calibration		
Poly gate	10	7	12	18
Local Interconnector	5	3	6	-
Contact 1	10	8	6	-
Metal 3	5	5	-	-
Via 2	10	N/A	-	-

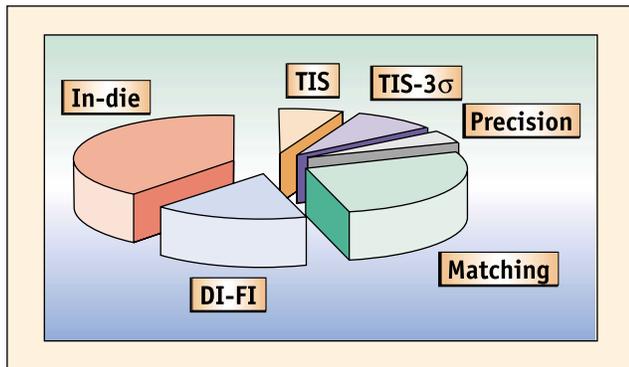Table 4. Summary of accuracy contributors.

Figure 11. Poly-level accuracy contributors.

scribe-line and in-die measurements of less than 18 nm indicate that both the pattern-size-dependent placement errors of the scanner as well as the processing impact on both the large metrology targets and the small device patterns are well under control. However, the magnitudes of lithographical effects such as pattern placement error strongly depend on the feature size. At the design rule of 0.18 μm, the impact doesn't yet seem to be critical. However, at least at the 100 nm design rule, with minimum features of 100 nm, and overlay budgets of 40 nm or even less, the pattern placement error may become an important contributor to the total overlay error. Bearing this in mind, one should reconsider the design of the scribe line overlay targets.

Acknowledgments

References

1. C. Gould, F. Goodwin, and W. Roberts, "Overlay measurement: Hidden error," Proc. SPIE 3998, pp. 400-415, 2000.
2. S-G. Bae, Y-K. Kim, K-Y. Park, J-S. Kim, W-G. Lee, S-W. Lee, and D-H. Lee, "The reduction of wafer scale error between DI and FI in multi-level metallization by adjusting edge detection method," Proc. SPIE 3998, pp. 460-469, 2000.
3. R. Seltmann, W. Demmerle, M. Staples, A. M. Minivielle, B. Schulz, and S. Muehle, "Overlay budget considerations for an all scanner fab," Proc. SPIE 4000, pp. 896-904, 2000.
4. A. Habermas, B. Ferguson, J. Seligson, E. Kassel, and P. Izikson, "Overlay accuracy – A metal layer study," these proceedings.
5. T. A. Brunner, "Impact of lens aberrations on optical lithography," IBM J. Research & Development, 41 (1997).
6. H. J. Levinson, Principles of Lithography, SPIE Press, Bellingham, WA, 2001.