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Digging Deep into High Aspect Ratio Process Control for Memory Technology

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Data is an integral part of our lives. Contrary to the past, where files had to be removed periodically to free up storage space, we now assume that our data will never be deleted. Why risk deleting the wrong file? Just keep them! This new approach consumes a lot of memory, and intensifies the demand for storage. Two of the main workhorses of the memory segment are NAND flash and DRAM. DRAM is dynamic, volatile and very fast, making it well suited for short term system memory. Conversely, NAND flash is non-volatile, which means it has good retention and can function well for long term low-cost storage. Higher speed, higher density and lower bit cost have been the main goals for both of these memory types as demand continues to increase.[1]

Reaching higher performance for NAND and DRAM has led each down a slightly different development path. Similar to logic, DRAM has continued the path of scaling to smaller cell designs. This dimension shrink has driven the introduction of multiple patterning technology and will eventually require EUV lithography in high volume manufacturing. Planar NAND was also facing scaling restrictions, and ultimately changed course to move in the vertical direction. This vertical integration has relaxed the lithography requirements for 3D NAND devices, and has instead migrated the most complex process challenges to deposition and etch.[2] The primary structure is created by alternating film depositions, then completing a high aspect ratio (HAR) etch through the entire stack. Each new node in 3D NAND takes the process to an even higher vertical stack. High aspect ratio structures have unique process control requirements since the channels are on the order of microns deep with angstrom-level requirements for precision.[3] Examples of these HAR structures are the channel hole in 3D NAND as seen in Figure 1, and the storage node capacitor found in advanced DRAM.

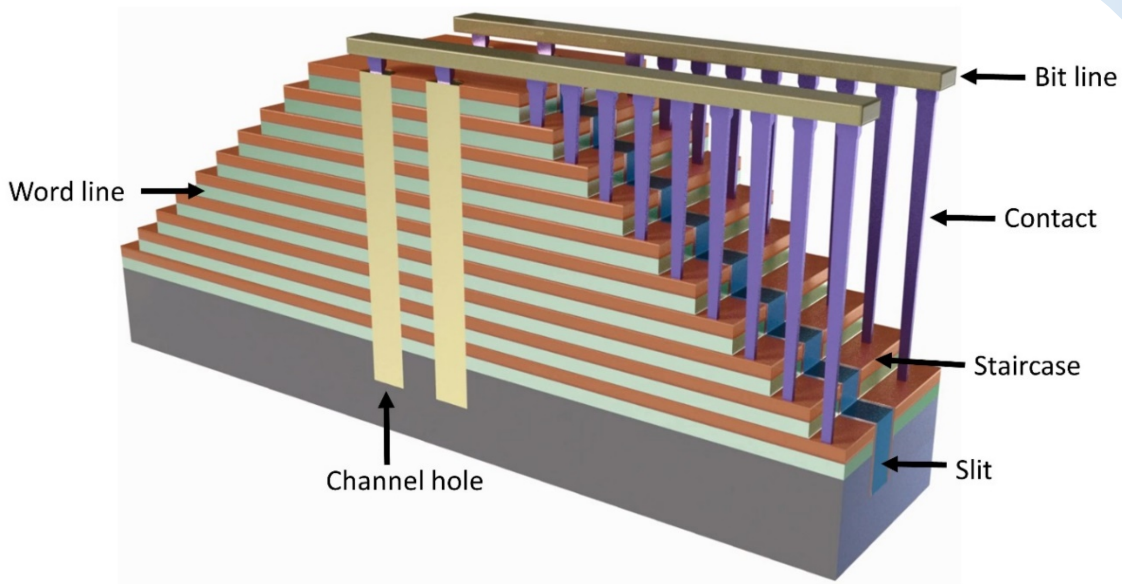

Figure 1. 3D NAND structure showing high aspect ratio (HAR) features such as the channel hole.

A few of the high priority process challenges with 3D NAND include channel hole and word line profile variability and defectivity, as well as shorts connecting the contacts to the staircase. DRAM challenges include storage node capacitor profile variability and defectivity, bit line defects and shrinking multi-patterning overlay error budgets. Refining the process for these deep narrow holes requires overcoming defectivity and profile challenges – to achieve yield during the development phase, and then ultimately improve and sustain the yield for high volume manufacturing. Some of these challenges have clear process control solutions, while others remain under development. Solving process issues in these complex stacks requires a multifaceted approach.

First line of defense -- Tool monitoring

When it comes to particle defects, it is always best to avoid them in the first place. At future patterning steps, particles can turn into yield limiting defects like bridges and opens. Avoiding defectivity is especially important for HAR stacks that include depositions of many layers in one process step, as with 3D NAND. A clean process tool will not drop a particle into the film stack. Therefore, ensuring process tool cleanliness is a proactive approach to avoiding buried particle defects. Unpatterned wafer inspection can monitor chambers at a high sampling rate to find

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any particle issues quickly. However, some defect mechanisms will manifest themselves only on patterned wafers; therefore, a well-rounded tool monitoring strategy includes sufficient sampling on patterned wafers as well.

Another important aspect of a comprehensive tool monitoring strategy is chamber monitoring. Temperature uniformity within a single etch tool, and matching between tools, are both important for maintaining a uniform etch profile across the wafer to keep the channel hole shape consistent. This uniformity is especially important for these micron-range etch processes since they have stringent angstrom-level precision requirements. Chamber temperature monitoring can be automated to compare current data to the baseline, and allow for quick corrections when a shift is detected.

In order for tool monitors to work effectively, process tool conditions should be as close to the production environment as possible. Temperature monitoring should be done in "plasma on" etch conditions, and unpatterned monitors should include a realistic film stack. Due to the complicated integration scheme of a product wafer, the tool monitoring strategy will need to be paired with a second line of defense that includes additional inline high sensitivity inspections and measurements.

Second line of defense -- Inline monitoring and control

Inline product wafers with HAR structures need monitoring for defects both at the wafer surface and below. Wafer inspection for defects on the surface of the wafer will help to find both particle and pattern type defects on surface layers.

Another process control issue for high aspect ratio wafer processing is wafer bowing. 3D NAND structures have alternating materials in the stack, creating a great deal of stress on the wafer. A thorough process-monitoring scheme will also need to monitor the bow and warp of the wafer to ensure it is still meeting specifications for downstream process steps.

What about buried defects in the HAR stack? Normally, wafer inspection can be done at multiple steps in the process to find defects at the source. However, the stack prior to the channel hole etch in 3D NAND is deposited in one process step, with no opportunity to pause the process for an inspection step. Ideally process engineers can avoid buried particles by keeping extremely clean process tools, but there will be integration related defects as well. Defects buried in the stack currently present a challenge directly detect at high throughput.

In the meantime, fabs are pursuing alternative inspection strategies for

defect detection. A buried defect can alter its surroundings, and cause a perturbation in the top pattern on the wafer. For the round channel holes, this perturbation may cause a ~10% change in critical dimension (CD), which is detectable by a high sensitivity wafer inspection system. Another inspection strategy to address buried defects uses a destructive etchback of the wafer to expose process issues such as under-etch defects, followed by a high sensitivity defect inspection.

In parallel to defect inspection, memory fab engineers deploy a variety of inline control strategies based on metrology, to investigate patterning topics such as profile, overlay and the process window. For both 3D NAND and DRAM, optical scatterometry measurements can provide limited structural information, but destructive lab techniques like TEM are the only methods of revealing the full profile shape. Non-destructive, fast measurements of the full HAR profile such as the channel hole or storage node capacitor are currently not available. Overlay requirements tend to be tighter for DRAM compared to 3D NAND since the storage node capacitor is built using double or triple patterning. Multi-patterning creates small dense features, which when paired with an aggressive HAR etch process, make it challenging to establish the process window.[4] This is an opportunity to apply the comprehensive process window discovery, expansion and control strategy shown in Figure 2, to help the fab team identify possible hotspot issues and effectively center their process window.[5]

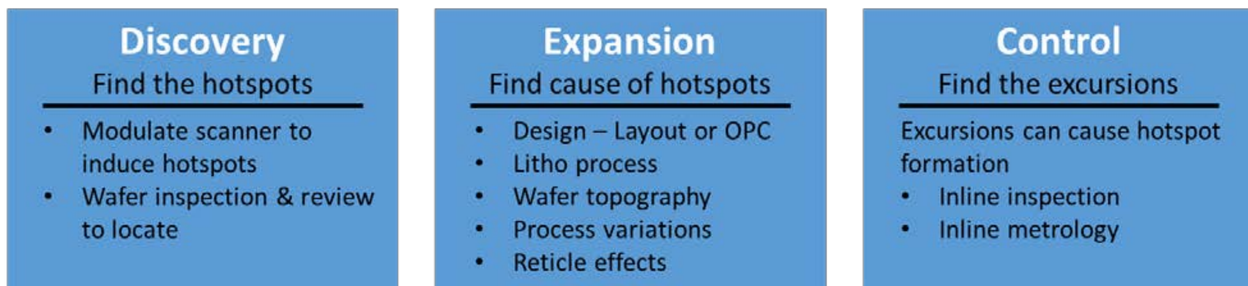

Figure 2. Process window discovery, expansion and control strategy. The first step is to identify the design- and process-related sources of hotspots; the second step is to expand the process window through fab-wide process improvements, and the third step is to implement inspection and metrology to detect and control critical process variations over time.

All of these measurements create a fab-wide stream of data, which must be combined with intelligent data analytics to drive both process control loops and efficient engineering analysis.

Don't forget the edge

HAR structures near the edge of the wafer tend to have the most process control issues. To obtain the maximum yield possible, fab engineers must emphasize monitoring and control of the wafer edge, imposing denser sampling compared to the rest of the wafer.

New Memory Technologies

3D NAND and DRAM continue to advance, as the stacks get higher, and the features continue to shrink. Additionally, the quest to combine the capacity, cost and non-volatility of NAND with the higher speed found in DRAM has resulted in many new forms of memory in development. These new kinds of memory include phase-change memory (PCM), ferroelectric RAM (FeRAM), spin-transfer torque magneto-resistive RAM (STT-MRAM), resistive RAM (RRAM or ReRAM) and more.[6]

With the new technology evolving with advanced nodes in 3D NAND and DRAM, and the new process flows associated with novel memory types, fabs will need to keep adapting their process control strategies to continue ramping and yielding advanced memory devices.

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