Advanced Lithography
Updates and Challenges for
Metrology and Inspection

Center for Semiconductor Research & Development
Advanced Lithography Process Technology Dept.

Tatsuhiko Higashiki
Contents

■ Device Roadmap and Lithography
■ Extendibility toward 1x nm hp and beyond with New Lithography
  ✓ EUVL
  ✓ NIL
  ✓ DSA
■ Conclusion
Contents

Device Roadmap and Lithography

Extendibility toward 1x nm hp and beyond with New Lithography

✓ EUVL
✓ NIL
✓ DSA

Conclusion
Rapid Increase of Information Volume Demand

All information that is created, captured, replicated and/or consumed by all humans on the planet.

\[1 \text{ZB} = 1,000,000,000,000,000,000,000 = 10^{21} \text{B}\]

All information is not fully stored, but partially stored. ⇒ Need for larger-capacity memory in the future.
Roadmap of the Memory

hp3xnm → hp2xnm → hp1xnm → hp0xnm

3D

BiCS

CP (Cross Point), etc
Lithography Challenges

More Moore

hp56nm  hp43nm  hp32nm  hp2xnm  hp1xnm  hp0xnm

ArF im
NA > 1 ~ 1.35

Light Source

EUVL NA0.32 → > 0.4x ?

Resist, Mask, Inspection, etc

EUVL + SADP

EUVL + DSA

Cost

ArF im SADP

ArF im SAQP/SAOP ?

ArF im SAQP + DSA

NIL

NIL + DSA

ML2

ML2 + DSA

Tool

Defect

Performance & Economics

SADP: self-aligned double patterning
SAQP: self-aligned quadruple patterning
SAOP: self-aligned octuplet patterning
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TOSHIBA
Leading Innovation

SADP: self-aligned double patterning
SAQP: self-aligned quadruple patterning
SAOP: self-aligned octuplet patterning
hp14nm Exposure was Realized by EUVL + SADP

Y. Watanabe et al, Photomask Japan 2010(April)
EUV Collaboration

TOSHIBA

Lithography
- Pattern Layout Tech. (OPC/DFM)
- Specification Design for Tools
- Mask process
- Resist process

Advanced EUVL
- Mask Quality
- Mask Inspections
- Resist Quality
- High NA Exposure

Suppliers
- Exposure Tool EDA
- Resist Material Mask
- Metrology and Inspection

Si Process

Device & design
**EUV Source Roadmap**

<table>
<thead>
<tr>
<th>Year</th>
<th>Source Model</th>
<th>HVM I</th>
<th>HVM II</th>
<th>HVM II</th>
<th>HVM II</th>
</tr>
</thead>
<tbody>
<tr>
<td>2010</td>
<td>HVM I</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2011</td>
<td>HVM I</td>
<td></td>
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<tr>
<td>2012</td>
<td>HVM I</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2013</td>
<td>HVM II</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2014</td>
<td>HVM II</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2015</td>
<td>HVM II</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**HVM I**
- 10 sources in operation
- 5 installed at Fabs
- 5 for development at Cymer / ASML

**HVM II**
- 1st source delivered
- Four in build

**EUV Source Power Roadmap**

<table>
<thead>
<tr>
<th>Source Model</th>
<th>HVM I</th>
<th>HVM II</th>
<th>HVM II</th>
<th>HVM II</th>
</tr>
</thead>
<tbody>
<tr>
<td>Average Laser Power (kW)</td>
<td>20</td>
<td>23</td>
<td>24</td>
<td>43</td>
</tr>
<tr>
<td>In-band CE (%)</td>
<td>2.0</td>
<td>2.0</td>
<td>2.5</td>
<td>3.0</td>
</tr>
<tr>
<td>Clean EUV Power (W)</td>
<td>60</td>
<td>80</td>
<td>125</td>
<td>250</td>
</tr>
</tbody>
</table>
“Let there be light” and there was light

"Fiat lux!" Et facta est lux.
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**MII’s Nano-Lithography Solution**

**Jet and Flash Imprint Lithography (J-FIL)**

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**Step 1: Dispense drops**

- 6025 photomask substrate

**Step 2: Lower imprint mask and fill pattern**

- Mask
- Planarization layer
- Substrate

**Step 3: Polymerize fluid with UV exposure**

- Planarization layer
- Substrate

**Step 4: Separate mask from substrate**

- Mask
- Planarization layer
- Substrate

---

**Major Advantages**

- Lower cost of ownership
  - No laser, no track, no lenses, no vacuum
- No resolution limit by optical projection system

---

**Step & Repeat or whole wafer imprinting**
Resolution of NIL Printing

hp16nm

Spot Beam

Template

Wafer

1 Month/Shot

VSB

Template

Wafer

hp24nm

Ref. T. Higashiki, 7970-02, SPIE 2011
CDU Update of MII Tool

- Imprinted-shots
- Measured-Metric (12 sites/shot x 20 shots/wafer)
- CDU(on wafer) 0.5 nm(3σ)
Mix and Match Overlay

Die by Die Alignment and Distortion Compensation

Low viscosity fluid

Substrate

Template

Magnification Compensation with Pressing Template sides

Template Resist

Alignment Mark

20-100nm

Achieving less than 10nm 3sigma Mix and Match overlay

Ref. T.Higashiki, 7970-02, SPIE 2011

<table>
<thead>
<tr>
<th></th>
<th>X</th>
<th>Y</th>
</tr>
</thead>
<tbody>
<tr>
<td>Raw Mean</td>
<td>-0.10</td>
<td>-0.63</td>
</tr>
<tr>
<td>Raw 3sigma</td>
<td>9.40</td>
<td>9.68</td>
</tr>
<tr>
<td>Mean + 3sigma</td>
<td>9.5</td>
<td>10.31</td>
</tr>
</tbody>
</table>
# Classification of Nanoimprint Defects

<table>
<thead>
<tr>
<th>Phenomenon</th>
<th>Example of Image</th>
<th>Countermeasure</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>1. Non-fill</strong></td>
<td><img src="image1.png" alt="Defect" /></td>
<td>Improvement of the filling process</td>
</tr>
<tr>
<td>Filling issue by remaining bubble</td>
<td><img src="image2.png" alt="Image" /></td>
<td></td>
</tr>
<tr>
<td><strong>2. Template</strong></td>
<td><img src="image3.png" alt="Defect" /></td>
<td>Improvement of template fabrication process</td>
</tr>
<tr>
<td>Printed template defect</td>
<td><img src="image4.png" alt="Image" /></td>
<td></td>
</tr>
<tr>
<td><strong>3. Plug</strong></td>
<td><img src="image5.png" alt="Defect" /></td>
<td>Improvement of separation process and materials</td>
</tr>
<tr>
<td>Separation issue, pattern is torn off</td>
<td><img src="image6.png" alt="Image" /></td>
<td></td>
</tr>
</tbody>
</table>
Electrical Test for Overall Evaluation

Test chip design

Open Test
snake pattern

Short Test
comb pattern

Open error

Short error
Improving Imprint Electrical Yield

**Electrical Defect Testing: Yield vs. Line Length**

- Steady progress in electrical yield of imprint process.
- Results are encouraging and improving with mask replica defect improvements.
# Current Status of NIL

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Target</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Template</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Master CDU</td>
<td>&lt; 1.0nm</td>
<td>1.2nm</td>
</tr>
<tr>
<td>Image Placement</td>
<td>&lt; 3nm(3σ)</td>
<td>2.5nm(3σ)</td>
</tr>
<tr>
<td>Master Defectivity</td>
<td>&lt; 0.1/cm²</td>
<td>0–1/cm²</td>
</tr>
<tr>
<td>Replica Defectivity</td>
<td>&lt; 1/cm²</td>
<td>~5/cm²</td>
</tr>
<tr>
<td><strong>Imprint</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LER</td>
<td>&lt; 2nm</td>
<td>2nm</td>
</tr>
<tr>
<td>CDU on Wafer</td>
<td>&lt; 1.0nm</td>
<td>0.5nm</td>
</tr>
<tr>
<td>Overlay Accuracy</td>
<td>&lt; 8nm</td>
<td>10nm</td>
</tr>
<tr>
<td>Defectivity (Short Wafer Runs)</td>
<td>&lt; 0.1/cm²</td>
<td>~2/cm²</td>
</tr>
<tr>
<td>Defectivity (Long Wafer Runs)</td>
<td>&lt; 1/cm²</td>
<td>50/cm²</td>
</tr>
<tr>
<td>Throughput</td>
<td>&gt;20 wph</td>
<td>10 wph</td>
</tr>
</tbody>
</table>
NIL Single Exposure by Mask Technology Revolution

**SADP**

- Litho.
- Slimming
- Film depo.
- etching

**NIL single**

- Mask (Template)
- Exposed

- Requires 20nm hp and beyond
  - High Resolution EB Writer and Resist
  - New Etcher and Repairing
  - New M&I

**Processed**
New Infrastructure for NIL Template

EB writer: “EBM8000”
(NuFlare)

Dry Etching Equipment: “ARESTM”
(Shibaura Mechatronics)

Scanning-type Developer: “PGSD”
Proximity-Gap-Suction-Development System
(Tokyo Electron)

- Slit and scan type development
- Narrow gap
- Suction slits for removing dissolution products

Special Structure for NIL template

- Extreme high uniformity of developing solution supply
- Nearly zero loading effect caused by dissolution products

http://www.nuflare.co.jp/product/ebm.html
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ArF im SAQP/SAOP?

Nil

Defect

Tool

ML2

NIL

NIL + DSA

ML2 + DSA

ArF im SAQP + DSA

More than Moore

Light Source

Cost

Performance & Economics

SADP: self-aligned double patterning
SAQP: self-aligned quadruple patterning
SAOP: self-aligned octuplet patterning
**DSA (Directed Self Assembly)**

**Change in Size**

- Spherical
- Cylindrical
- Bicontinuous
- Lamella

**Composition**

- B polymer
- A polymer

**Change in Structure**

- Hydrophilic
- Hydrophobic

**Chemical bond**

**DSA Molecule**

**Micro-Phase Separated Structures of Block-copolymer**

DSA for Dense Pattern

BCP: block co-polymer

Hydrophobic

Hydrophilic

Acrylic styrene

Under layer with guide pattern

Coating

Heating and phase separation

BCP aligns with guide pattern
Grapho-Epitaxy & Chemo-Epitaxy


Tada, Macromol. 41,9267(2008)
**DSA for Contact Hole**

**Process Flow of DSA Lithography**

1. **BCP Coat**
   - BCP
   - Guide

2. **Annealing**
   - Hydrophilic
   - Hydrophobic
   - DSA

3. **Development**
   - 100 nm
Guide Hole vs. DSA Hole

Guide hole

Ave. CD 72.1nm
3sigma 7.6nm

DSA hole

Ave. CD 28.5nm
3sigma 1.3nm

Ref. Y. Seino, SPIE Advanced Lithography 2012 8323-33
Hole Open Yield

100% yield on 300mm wafer center!
**DSA OPC/DfM/APC Flow**

**OPC**
- EDA Tool
- Guide Data
  - OPC Spec/Verification 5x?
  - Sim TAT x 10k
  - Accuracy x 20
- Condition (material/process)
- Judge
- 3D Metrology & Inspection
- Wafer Process

**DfM**
- Model
- DSA Simulation
- HotSpot result
- FeedBack
- EDA Tool

**APC**
- FeedForward
MINDMAP® for Engineering Challenges of DSA Computational Lithography

3D Etching Sim for DSA
Etg Model
TCAD System

Guide Pattern
Hole/ L&S
Grapho/Chemo
DFM/ DR

OPC/DFM
- Tradeoff
TAT/ accuracy

DSA Simulation
Molecular design
Microphase separation

Microphase separation:
 msec～sec order

Big Difference Exists!!

Sim time step
MD: nsec
Coarse Graining: 100 nsec
SCF: usec?
more approx. model:

Issues
Prediction accuracy
Sim TAT Verification

Target
0.25n @hp7nm
1min/10um² 5hr

Current status
5nm
5hr

Root Causes
Model inadequateness
MD/DPD/SCF
Parameter uncertainty

Solution
R&D Collaboration
with Univ/Institution,
about
Model innovation
Measurement,
Computer science

Verification
Compare to wafer
to design
M&I: how?/what?
Spec?

Empirical Model

HW acceleration
FPGA/ GPU

HW acceleration
FPGA/ GPU
### DSA Simulation Model

**Model**

<table>
<thead>
<tr>
<th>Methodology</th>
<th>Self Consistent mean Field</th>
<th>Dissipative Particle Dynamics</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Based on statistical field theory</td>
<td>Based on Newton's motion equation</td>
</tr>
<tr>
<td><strong>Challenge</strong></td>
<td>Modeling of thermal fluctuations</td>
<td>Difficult to fit to a measured data</td>
</tr>
</tbody>
</table>

**Speed**

- **TAT**: (1m/10μm²)
- **Prediction Accuracy**
  - Shroedinger's Equation etc
  - Rigorous Model
  - Impractical model
  - (<0.25nm)
  - (5nm)

**Target**

- **TAT**: (? years/10μm²)

*Needs drastic improvement!!*
Example of DPD Simulation

**DSA Simulation Model**

- Molecular Dynamics
- Coarse Grained Model by DPD (Dissipative Particle Dynamics)

Available Free Software Tools are: LAMMPS/GROMAX/OCTA-COGNAC,

\[ m_i \frac{d^2 r_i}{dt^2} = F_i = \sum_{j \neq i} (F_{ij}^S + F_{ij}^C + F_{ij}^D + F_{ij}^R) \]

- Repulsive Force
- Dissipative Force
- Brownian Motion

PS-b-PMMA

Top-down

Top

Sidewall

Bottom

X-section
## Metrology for DSA 3D Profile

<table>
<thead>
<tr>
<th>Tool</th>
<th>TEM</th>
<th>XSEM</th>
<th>AFM</th>
<th>CD-SAXS</th>
<th>OCD</th>
</tr>
</thead>
<tbody>
<tr>
<td>Method</td>
<td>Imaging tool</td>
<td></td>
<td></td>
<td>Diffraction tool (image is derived from computation)</td>
<td></td>
</tr>
<tr>
<td>Application</td>
<td>•Resolution</td>
<td>•Resolution</td>
<td>•Non-destructive</td>
<td>•Non-destructive •Frequency analysis •Simple model</td>
<td>•Non-destructive •Monitor internal structure •High throughput</td>
</tr>
<tr>
<td>Concerns</td>
<td>•Destructive •Sample damage</td>
<td>•Destructive •Sample damage</td>
<td>•Only surface topography •Resolution</td>
<td>•Only surface topography •Target size</td>
<td>•Model complexity</td>
</tr>
</tbody>
</table>

- **TEM, XSEM and SAXS** are required for DSA material development.
- **OCD** is effective for process window analysis and SPC/APC
Challenges for DSA Lithography

• High performance DSA material
  – Resolution
  – LWR/LER
  – Etching
• Long term stability
  – Robust material and tool for environmental control such as surface energy stability, temperature, humidity, pressure and PH, etc.
  – Defectivity, CD and overlay accuracy
• Development of molecular dynamics based DSA simulator
  – More accurate simulation model
    • BCP and related molecular design
    • Microphase separation (2D/3D)
    • DSA and guide patterning (litho/wet/dry)
  – TAT vs accuracy trade-off
• DSA OPC/DFM technology
  – Design rule verification
• Metrology & Inspection
  – Metrology for 3D profile
  – Inspection technology for 1xnmhp and beyond needs to overcome t-put vs accuracy/sensitivity trade-off.
Key Challenges for Shrinking

Metrology & Inspection technologies should be prepared for NGL?
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Conclusion

- EUVL
  - We are waiting EUVL for HV production.
  - Light source performance is a significant concern.

- NIL
  - NIL performance has been improving as alternative lithography for next generation devices to reduce process cost as well as pattern size.

- DSA
  - DSA will be a complementary technology for all other lithography.

◆ Next Challenges
  - Single exposure NIL will be enabled by mask(template) technology revolution.
  - Next generation lithography will depend on innovation of infrastructure technologies such as OPC, DFM, M&I, etching and cleaning.