Demonstration of Lithography Patterns using Reflective E-beam Direct Write

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ABSTRACT

Traditionally, e-beam direct write lithography has been too slow for most lithography applications. E-beam direct write lithography has been used for mask writing rather than wafer processing since the maximum blur requirements limit column beam current - which drives e-beam throughput. To print small features and a fine pitch with an e-beam tool requires a sacrifice in processing time unless one significantly increases the total number of beams on a single writing tool. Because of the uncertainty with regards to the optical lithography roadmap beyond the 22 nm technology node, the semiconductor equipment industry is in the process of designing and testing e-beam lithography tools with the potential for high volume wafer processing. For this work, we report on the development and current status of a new maskless, direct write e-beam lithography tool which has the potential for high volume lithography at and below the 22 nm technology node.

A Reflective Electron Beam Lithography (REBL) tool is being developed for high throughput electron beam direct write maskless lithography. The system is targeting critical patterning steps at the 22 nm node and beyond at a capital cost equivalent to conventional lithography. Reflective Electron Beam Lithography incorporates a number of novel technologies to generate and expose lithographic patterns with a throughput and footprint comparable to current 193 nm immersion lithography systems. A patented, reflective electron optic or Digital Pattern Generator (DPG) enables the unique approach. The Digital Pattern Generator is a CMOS ASIC chip with an array of small, independently controllable lens elements (lenslets), which act as an array of electron mirrors. In this way, the REBL system is capable of generating the pattern to be written using massively parallel exposure by ~1 million beams at extremely high data rates (~ 1Tbps). A rotary stage concept using a rotating platen carrying multiple wafers optimizes the writing strategy of the DPG to achieve the capability of high throughput for sparse pattern wafer levels. The lens elements on the DPG are fabricated at IMEC (Leuven, Belgium) under IMEC’s CMORE program. The CMOS fabricated DPG contains ~ 1,000,000 lens elements, allowing for 1,000,000 individually controllable beamlets. A single lens element consists of 5 electrodes, each of which can be set at controlled voltage levels to either absorb or reflect the electron beam. A system using a linear movable stage and the DPG integrated into the electron optics module was used to expose patterns on device representative wafers. Results of these exposure tests are discussed.

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1. INTRODUCTION

The REBL program aims to develop a novel, high throughput, maskless lithography system. The program at KLA-Tencor is jointly funded by KLA-Tencor and DARPA, under the Maskless Nanowriter Program. The program is specifically targeting five to seven wafer layers/levels per hour at the 45 nm node. The system is being designed however, for extension to the 22 nm node and beyond. Figure 1 shows a schematic diagram of the current REBL system. Electron Beam Lithography (EBL), since its beginning, has fallen short in lithography for High Volume Manufacturing (HVM) because of insufficient throughput - except for mask making. High resolution lithography and customization for specialized products are other areas where electron beam direct write (EBDW) has proven useful. For these applications both resolution and maskless imaging have been more important than throughput. Quick-turn-around and small lot manufacturing have also proved to be quite successful applications of EBDW. SCALPEL and PREVAIL were two competing electron projection lithography programs that demonstrated very good progress but did not utilize one of EBL’s most important assets, namely, maskless imaging. Currently, there are three major maskless EBDW programs under development: MAPPER, IMS, and REBL. The REBL program will eventually target sub-20 nm lithography at a capital cost equivalent to conventional lithography. Future system designs should allow for high wafer throughputs and footprints comparable to current 193nm immersion lithography systems.

2. SYSTEM OVERVIEW

The REBL architecture has at its foundation the concepts of reflective electron optics and a multiple wafer rotating stage. The reflective optics approach was chosen because of the compact form while still generating a million beamlets in a single column, even though this limits the usable beam current to single digit microamperes due to beam blur from Coulomb interaction between electrons. It was determined that this was a reasonable trade-off when other system issues are taken into consideration. Some of these other system issues are calibrations, sensitivity to electromagnetic interference, heating effects, data path architecture, and electron optics field of view. The rotary wafer stage allows the REBL system to perform at high throughput with a minimum number of mechanical distortions. It also is a convenient architecture for beam positioning and diagnostics. This architecture, along with specially designed positioning sensors, helps ensure that the system has the positioning accuracy necessary for the stringent CD uniformity and overlay budgets for the 22 nodes.

Figure 1 shows an overview of the REBL system concept. The key advantages of the REBL architecture besides the above mentioned ones are: dose proximity correction on a pixel by pixel basis, pixel exposure redundancy, Time Domain Integration (TDI) exposure, the use of a compact writing area, and 50 to 100 KeV exposure energies. The dose proximity correction, controlled by the reflective optical element of 1 million pixels, allows for sub-pixel edge placement and nanometer-level CD control. Due to the high number of parallel beams and the writing strategy, the REBL system can employ a strategy in which it does not need to use all of the available pixels. This pixel exposure redundancy ensures that each wafer pixel is exposed by a minimum of 8 different DPG pixels. The writing strategy is based on proven TDI exposure architectures, allowing for writing on a continuously moving stage for minimal stage overhead. The small writing area minimizes blur and placement errors from across-swath distortions like thermal expansion, differential magnetic fields, power supply drift, and stage yaw. The design also allows for real time, as needed, correction.
of global wafer expansion. The 50 to 100 KeV exposure energy enables high aspect ratio patterning of resist for simple processing and minimizes charging-induced placement errors.

![REBL concept diagram](image)

**Figure 1.** REBL concept diagram

### 3. DIGITAL PATTERN GENERATOR

Key to the performance of the REBL system is the digital pattern generator, DPG. The DPG is a CMOS ASIC chip with an array of small, independently controllable electron mirrors in an array producing over 1 million beamlets. This array of electron mirrors is analogous to the DLP® technology used by Texas Instruments for projection television. The concept of massively parallel and individually controlled beamlets reflected from the DPG is the principal enabling technology that provides the high speed maskless pattern generation capability. Producing an effective electron mirror, however, proved to be more difficult than first envisioned. This required an extensive development effort to integrate the CMOS logic with a microelectromechanical systems (MEMS) structure that produces the required performance.

REBL’s reflective technology involves illuminating an array of small electrodes on the DPG with low energy electrons that have been decelerated to ~1 eV. A small negative bias is applied to the entire mirror array, creating sufficient repulsive force in the region immediately above the electrodes of this array to reflect the electrons, which illuminate it back into a region where they are reaccelerated. A small positive potential is applied to some electrodes, which absorb the portion of the illumination beam that strikes them. The pixels are digital; they are either on or off. The DPG was originally constructed as a small array 256 x 256 of 4µm x 4
µm metallic pads separated by a 0.4 µm gap as a proof-of-concept test. This array was intended to form a reflective spatial modulator that produces an array of electron beams individually controlled to produce a patterned electron beam.

It was known that a flat array of mirrors would not work perfectly because every mirror when turned on or off would affect the potential of every mirror in its vicinity, that is, it would experience "cross-talk" with neighboring mirrors. Actually, this cross-talk effect was observed to act over a considerable distance. In addition, it was desirable to greatly increase the electric field near the mirror surface. In front of the DPG is a large electrostatic lens referred to as the DPG lens, with the DPG forming a potential boundary at one end. The electrostatic DPG lens serves a dual purpose: it forms a virtual image of the crossover at infinity and it decelerates the electrons to within a few volts of the cathode potential near the mirror array's surface. When a mirror is turned on at the DPG, it will reflect electrons from the illuminating beam. These reflected electrons are reaccelerated back toward the wafer as they travel through the accelerating field of the electrostatic DPG lens.

Because this DPG lens is very large, 50–100 mm², the electric field is relatively weak. The electrons reflecting off the mirrors have an energy spread near 1 eV. This means that the electrons will reflect not from a plane, but from a region of tens of micrometers above the mirror surface. A development effort was started early in the program to develop a means of eliminating the cross-talk problem and increase the electric field near the mirror. The result of a nearly 3 year effort was a MEMS structure, which formed an array of microlenses - one set for each mirror. Each of these lens stacks is referred to as a lenslet, comprised of a set of five electrodes (referred to as a pentode) separated by four dielectric layers (Figure 2). The top electrode interfaces with the macro-electron optics of the DPG lens. The top electrode and the next three electrodes (named upper, middle, and lower) are common to all the lenslets of the array. The bottom electrode is the mirror that is switched on or off individually by means of the CMOS DPG chip located below the lenslet array.

The fabrication of the lenslet array was a major effort since the complete pentode structure required over 75 custom MEMS processing steps, including the use of novel processing to perform high-aspect ratio etching. The lenslet array MEMS structure was developed independently from the CMOS development by IMEC, the Inter-University Microelectronics Consortium, in Leuven, Belgium. IMEC was chosen to fabricate the lenslet device because the facility offers a wide range of semiconductor and MEMS manufacturing services and process expertise. The entire development of this lenslet array was carried out using a 300 mm wafer tool set at IMEC’s 300 mm fab. Fabricating the lenslet MEMS on 300 mm wafers was required because the CMOS logic was also fabricated on 300 mm wafers and the lenslet MEMS is integrated with the CMOS DPG chip as one chip. A relatively simple quasistatic design of a DPG chip was used during the course of the development of the lenslet MEMS.
The latest lenslet MEMS comprises a 4096 x 248 array of electron optical lenses each 1.4 µm in diameter and arranged on a 1.6 µm pitch, which matches the pitch of the CMOS array of mirror control pads. The lenslets were designed through extensive electron optic simulation in conjunction with the fabrication process (as it evolved) to produce a lenslet design with high electron reflection efficiency and contrast. For development purposes, the lenslet structure is wired to address each of the 248 columns - comprising 4096 lenslet pixels. This wiring simplification allows for the demonstration of a one dimensional array of lines and spaces with varying numbers of pixels in width. The process flow (Figure 3) developed by the team at IMEC was designed to optimize the electrode-to-electrode alignment while maintaining a high aspect ratio. The process flow comprises lithography and etch steps for each lenslet electrode, with a final etch step to clear the dielectric out of the lenslet holes. To ensure good uniformity of all parameters, several metrology steps are included in the process, resulting in a 75+ step process flow. To ensure high efficiency of the lenslets, two key criteria need to be met: 1) good alignment between the 5 electrodes and a 2) a high aspect ratio hole.

Figure 4 shows the simulated change in efficiency of a single lenslet as a function of the offset between the central axes of two electrodes. The steep drop-off in efficiency requires that all electrodes are aligned to one another within several nm. Both the alignment and aspect ratio requirements are difficult to meet even with state of the art MEMS processing and resolving these issues consumed a significant percentage of the long process development time.

There are two potential process flows for creating the lenslet structure. The first one is to deposit all layers in sequence and perform a single etch through all layers to form the high aspect ratio lenslet. This process flow has the advantage that it will automatically align all electrodes to one another. The disadvantage is that all complexity is moved to the final etch process. Since the lenslets consist of electrodes separated by dielectric materials, this would require an etch process that can etch both dielectric and metal materials. We have tried to develop this process flow but were unsuccessful in developing a robust etch process. We were not able to achieve the required uniformity and aspect ratio with this process sequence. Each etch that fully etched the hole resulted in a severely damaged top electrode and taper, making the lenslets non-functional. When backing off the etch strength in order to preserve the top electrode and the desired taper of the holes, we were unsuccessful in etching all the way to the bottom of the electrode stack. The second method is to etch each metal layer individually, prior to depositing the next layer. This sequence creates a stack of metals with holes, filled in by the dielectric that is used to separate the electrodes. There are two disadvantages of this method.
The first is the increased number of process steps, including extra lithography and etch steps, as well as CMP and overlay measurement steps. The second disadvantage is that this puts very stringent requirements on the metal hole tech process, since each hole needs to be accurately aligned to the next. To resolve this potential problem, the litho steps were all performed on a single scanner, and dummy wafers were used to feed forward overlay information to the final device wafers. Resulting alignment is show in figure 5. The final hole etch needs to etch only a high aspect dielectric layer, and we have demonstrated good etch uniformity across the active lenslet array.

![Figure 3. Simplified pentode (lenslet) process flow](image-url)
Figure 4. Simulated sensitivity to electrode alignment. DZ is offset between the axes of two concentric electrodes.

![Graph showing sensitivity](image)

**Figure 4.** Simulated sensitivity to electrode alignment. DZ is offset between the axes of two concentric electrodes.

Figure 5. Electrode alignment after optimization of the process.

The resulting lenslets, as shown in the cross section in Figure 6, meet all the requirements stipulated by the performance specs. Due to the high degree of process uniformity, the REBL system is able to utilize the one million lenslets as designed. Due to the redundancy in grey level pixels, not every lenslet has to be functional, as long as the reflection non-uniformity is less than 10%.
The next step is to integrate the developed lenslet process onto the previously created CMOS. Our CMOS chips were made at TSMC using their standard 65nm process. After creation of the CMOS, the wafers were further processed at IMEC in their 300mm fab. To integrate the above described process onto 65nm CMOS, several process steps needed to be developed. These include alignment of the MEMS structure to the underlying CMOS and creating electrical connectivity between the MEMS structure and the CMOS circuits. At the current state of our program we have proven that the integration between CMOS and MEMS structure is successful. This was demonstrated initially with cross sections, indicating alignment between the CMOS pads and the corresponding MEMS elements. Electrical test structures build into the lenslet process were used to test basic electrical contact between the top metal of the CMOS and the lowest metal layers of the MEMS structure.

The integrated MEMS on CMOS chips were bonded in special test packages and we have been able to demonstrate that the electrical performance of the chip with and without the lenslet process steps is equivalent. We have tested this by pushing data through the CMOS and measuring bit error rates. A photograph of the resulting bonded chip is shown in figure 7. We are now working on developing a repeatable bonding process for bonding the chip onto our vacuum compatible package. Bonding to a device with as many leads as ours has proven difficult, but we expect to have resolved this in the next few months.
In addition to the above discussed subsystems, the optical alignment system is vital to the performance of the REBL system. The currently used optical sensor is based on KLA-Tencor’s proven overlay technology. The advantages of this system include a relatively low cost platform that allows for high speed and high precision measurement of pattern positions on wafers during exposure – using overlay marks (Figure 8). The technology leverages KLA-Tencor’s extensive experience in overlay metrology. The optical alignment system acquires mark location optically, “on-the-fly”, as the wafer moves. This method allows for the correction of position changes during the print cycle, caused by temperature and other effects. The current system enables mix and match alignment with optical lithography. Current results demonstrate capability for sub-nanometer mark acquisition precision.
5. HOW TO ACHIEVE THROUGHPUT FOR HVM

The question for direct write e-beam is how to best achieve the throughput required for a high volume lithography tool. A single REBL column will not provide the throughput needed for High Volume Manufacturing (HVM). Therefore, a multiple column architecture will be employed to increase the total throughput without putting unphysical requirements on the column architecture. The rotary stage platform offers a convenient system for multiple columns, with enough space for both a large number of columns as well as integrated beam diagnostics and position control systems. We are currently working to optimize the overall system architecture (Figure 9 below).

As the number of columns increases many other system requirements are significantly reduced. A larger number of columns allows for a slower writing speed per column, reducing the requirements on current through a single column and stage speed. The key, then, is to make the optics small, simple, reliable, and inexpensive enough to replicate many times per lithography platform. KLA-Tencor is working on multi-column concepts which fit this strategy. Increasing the number of columns allows for concentrating complexity into systems that scale, like the DPG design, rendering algorithms, and stage and beam positioning algorithms. The DPG leverages CMOS technology and infrastructure, which should scale with device node. The rotary rendering algorithms leverage HPC (High Performance Computing) infrastructure, which will also improve with progressive design shrinks. The REBL stage control and beam positioning algorithms leverage HPC, DSP (Digital Signal Processing), and FPGA (Field Programmable Gate Array) technologies. By contrast, elements which are traditionally complex in lithography systems are comparatively simple; for example the optics, stage, and source are all readily available. Figures 6a-6b show a proposed architecture consisting of two blocks of six columns on a single platform. Several platforms are clustered together and connected to a single track system to achieve the required HVM throughput.

Figures 9a-9b. REBL CAD examples for HVM with multiple columns

6. CURRENT STATUS

At this time in the REBL program the team has designed, assembled, and tested the first two iterations of the optical column. Column 1 has been integrated on a linear stage platform to test printing
performance without the overhead of a rotary stage. All subsystems have been tested and perform to specification. This includes all systems needed for position and beam control, including the stage, stage metrology and control, and the wafer metrology system. Using the first e-beam column the team has demonstrated initial lithography performance. Images have been produced using both PMMA and CAR. The selected CAR has a sensitivity of better then 18 µC/cm² for features down to 45 nm. Using this resist we have demonstrated 65 nm lines in CAR (Figure 10a).

The second column, Column 2, has been up and running for several months on a specially designed test stand. This test stand includes an electron microscope and a scintillator screen to re-magnify and capture the wafer plane image. This allows us to test e-beam performance at the wafer plane without the influence of resist. We are currently characterizing the column’s performance and testing DPG’s. Column 2 is performing as expected and the image below shows that we can individually resolve pixels on a 25.6 nm pitch (Figure 10b). We are planning two more iterations of columns in the near future. The first iteration, Column 3, is currently being assembled and is designed to improve the minimum resolution. The next column will be designed with the same optical principles, but using the previously mentioned techniques for reducing column size.

![Figures 10a-10b; (L) REBL CAR exposures, (R) DPG pixel images](image)

7. SUMMARY

The design, implementation and improved performance of current REBL system was reviewed. Evolutionary progress of the column design is expected to produce a column that can deliver several wafers per hour. A new design that dramatically reduces the size of the column will enable a multiple-column architecture. With a multi-column approach, it is possible to obtain throughputs of multiple tens of wph at the 22 nm node with a single platform. Even though this number will decrease as the node decreases, when EBDW is used, as expected for patterns having much less than 50% coverage, the throughput will improve proportionally. In additional, multiple platforms will comfortably meet the footprint and cost constraints set by traditional lithography systems.

A lenslet MEMS structure has been under development for nearly 3 years and has now been successfully integrated with the CMOS DPG chip. Together with our partners and suppliers, we have successfully designed and manufactured a high efficiency, high contrast electron mirror with low voltage switching of the
one million individually-addressed beamlets. Efficiencies of 30% have been achieved so far with switching voltages of a few volts. A discussion of the key success parameters and how these were met was the main focus of this paper. We believe that we now have a proven solution to our digital pattern generator concept and have used this to demonstrate initial static exposures, down to 65nm in CAR. The remaining open item is the development of a reliable bonding process for our DPG chip onto a vacuum compatible carrier. We are making progress towards resolving this issue in the near future. The plan is to use this CMOS chip with integrated MEMS structure to demonstrate our dynamic writing strategy.

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REFERENCES