ABSTRACT

Reticle quality and the capability to qualify a reticle are key issues for EUV Lithography. We expect current and planned optical inspection systems will provide inspection capability adequate for development and production of 2X HP masks. We illustrate inspection technology extendibility through simulation of 193nm-based inspection of advanced EUV patterned masks. The influence of EUV absorber design for 193nm optical contrast and defect sensitivity will be identified for absorber designs of current interest.

Keywords: Mask Inspection; EUV Lithography;

1. INTRODUCTION

1.1 Lithography drivers in the semiconductor industry

Lithography technology development to support continued scaling in the semiconductor industry continues along the main options of 193nm-based Immersion, EUV Lithography (EUVL), and NanoImprint (NIL), all of which require distinctly different masks, as well as direct-write electron beam methods. For mask inspection system development and application, the diverse forms of masks associated with these options present a unique challenge to the flexibility of current and future system optical designs. When EUV Lithography transitions from the first scanner generation (0.25 NA imaging) to the resolution provided by 0.32 NA optics, pattern densities on EUVL masks will move to low 2X nm HP (wafer scale).

1.2 Inspection System technology development

KLA-Tencor recently introduced the first generation of a 193nm-based inspection platform, with product name Teron™. The platform is expressly designed to provide broad capability and thus serve well the industry’s changing needs. As part of the effort to extend the Teron platform capability through the 22nm HP node, we have studied using simulations the inspection performance on EUVL masks, and have begun to assess experimentally both current system inspection performance, as well as potential future configurations. In this report we provide a snapshot of ongoing research centered on EUV mask absorber material design and its optimization, which illustrates both the challenges and the opportunities involved.

2. EUVL MASK MATERIAL OPTIMIZATION

2.1 Optimizing Fabrication

In the early stages of EUVL mask optimization, absorber material candidates were screened for basic imaging and fabrication properties.1,2 A consensus has emerged around TaN-based designs. Recently, EUVL mask optimization has focused on improving the EUVL process window for both binary and EPSM style absorber designs.3,4

2.2 Simultaneous Optimization including Inspection and Metrology Criteria

The insertion of EUVL into high volume manufacturing (HVM) will benefit if the mask design optimization process is broadened to take into account the 193nm inspection performance, analogous to prior optimizations performed for 257nm-based inspection systems.5 Inspection-related optimization must build upon prior learning, and be compatible and consistent with fabrication and process window optimizations, as illustrated in Fig 1.

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It is important to identify early the preferred optimal solutions, and their potential dependence on pattern type (eg., L/S vs Contact), so as to provide the lead time for sufficient fabrication and test learning cycles prior to the relevant HVM ramp. Accordingly, we are engaged in prototype fabrication and experimental inspection studies with mask shops of early EUVL adopters.

In Figure 2 we illustrate one goal of this research effort by showing an illustrative example of the dependence of image contrast on pattern pitch, optical configuration, and absorber film stack material choice. The particular performance metric chosen for the illustration, image contrast, is one of several inspection performance metrics that must be considered simultaneously. Traditionally, image contrast is a necessary but not sufficient performance metric in mask inspection applications. Other metrics include defect signal-to-noise ratio (SNR), and depth of focus.

Conceptually, image contrast for a 1D pattern can be enhanced by use of off-axis illumination. This optical enhancement might provide inspection capability which enables production inspection well into the 2x nm HP regime.
To achieve further enhancements, thin cap layers applied to the absorber, which enhance or suppress the 193nm local reflectivity, might result in additional image contrast, and enable inspection capability deep into the 2x nm HP node. Since the 193nm wavelength light illuminates quasi-periodic mask features with a pitch and depth comparable to the wavelength, the dependence of image contrast and defect SNR on imaging conditions is not simple or obvious, and rigorous electromagnetic simulation methods must be employed to obtain diffraction efficiencies for the propagating modes.

2.3 Screening of Mask Absorber Materials and Designs

A number of absorber designs have been considered historically, and, for completeness, in our survey. Figure 3 shows a sample of designs we have screened for inspection performance. The conventional absorber is just bare TaN, while we use the “booster” label for a design in which a thin cap layer is applied to enhance absorber reflectivity at 193nm. For suppression of reflectivity at 193nm, an anti-reflective coating (ARC) is applied on top of the absorber. “Inverted” absorber designs apply an ARC to the multi-layer regions in addition to the high reflectivity cap on the absorber. “Embedded” and “Etch-away” absorber designs are self-explanatory. Although we have noted attractive inspection performance for some alternatives, mask manufacturing or lithography process window considerations block their use, and are accordingly marked “not viable”. In the rest of this paper, we will show results for bare, “booster” (HR cap), or ARC designs.

Although thicker designs (65-80 nm TaN height) are still prevalent, largely driven by considerations of horizontal-vertical bias, an industry consensus has formed around the choice of TaN absorber height in the neighborhood of 50nm, and that is the value we have adopted for the baseline configuration in our extensive rigorous simulations of mask diffraction under 193 nm illumination.

![Scheme #1 – Enhance Absorber Reflectivity at 193nm](image1)

![Scheme #2 – Reduce Absorber Reflectivity at 193nm](image2)

Figure 3. Absorber options considered for EUV Mask material designs.

3. SIMULATION METHODS

To compute diffraction efficiencies, we employ PROLITH™ Ver. 12, as well as various custom propagation and imaging codes. Figure 4 shows the absorber stack geometries and material properties assumed in this study. Material properties depend on deposition and processing conditions, which are likely to vary, indicating the importance of experimental studies for conclusive work.
To illustrate the simulation methodology, Figure 5 shows an example of two simulation runs, for ARC and “Booster” absorber designs, in which the image contrast for a unit cell is measured as the half-pitch is swept from 23 to 50 nm (wafer scale). Contrast reversal is evident for the ARC design, while the booster design at large pitch shows a behavior in which contrast is driven by phase effects, but has an improved contrast relative to ARC in the small pitch regime.

Figure 5. Example of Image Intensity modulation in a 1:1 Line/Space unit cell for two absorber material designs, as the wafer scale half-pitch (HP) is swept from 23 to 50 nm.

4. SIMULATION EXAMPLES AND RESULTS

4.1 Optimizing Image Modulation for 1:1 Line/Space geometry

Full optimization of system performance requires examination of the inspection performance on a wide variety of pattern geometries, as well as defect types. For brevity, in this report we focus on 1D patterns, with two classes of defect types. As noted above, multiple inspection metrics must be considered for each instance of pattern and defect. Again, for brevity, here we show examples for base pattern image modulation (contrast), and defect SNR metrics. We show first an example of the behavior of image intensity modulation (contrast) under conventional imaging conditions. By conventional we mean illumination pupil fill which is full or almost full, and for unpolarized or circularly polarized illumination. The optical configuration parameters used in this study are either close to those currently employed by the Teron platform or capable of insertion in the near-term Teron roadmap.
Figure 6 summarizes the line-width dependence (i.e., thru-pitch behavior) of three absorber designs under conventional imaging conditions, supplemented by a “thin-mask” model for reference. To facilitate comparisons across absorber designs, the modulations across all designs are normalized by the value for the data point indicated.

Departures from the thin-mask model are significant. We find that absorber choice has a substantial impact on image modulation. Under conventional imaging, it appears that the ARC-based scheme is not desirable for patterns dominated by 1D geometry, if the inspection system performance depends significantly on the pattern contrast. Although ARC-based absorber designs for EUV masks have previously performed well for 257nm illumination and larger pitches, it is not obvious that the ARC-based design paradigm will persist under 193nm illumination of much smaller pitch values.

Off-axis illumination (e.g., dipole) is routinely employed in lithography to improve imaging performance without changing numerical aperture (NA) or wavelength of illuminating light. Figure 7 shows the image modulation for 1:1 L/S geometry as a function of pitch for off-axis illumination conditions, for the same absorber designs, as well as the thin-mask model.

Once again, departures from the thin-mask model are significant. Similar to the behavior under conventional illumination, the ARC-base design under off-axis illumination conditions presents much smaller modulation at small values of line width, while the booster and bare TaN (conventional absorber) designs offer significantly greater image modulation.

Figure 6. Image modulation for 1:1 L/S geometry versus wafer scale Line Width (nm) using conventional image configuration, for various absorber material designs.
4.2 Example of optimizing defect signals

For a particular class of 2D defects in a 1D pattern, intrusions (missing absorber), Figure 8 shows the trend of defect contrast as a function of 1D half-pitch, for both conventional and off-axis illumination modes. Defect contrast is estimated as the ratio of the magnitude of the difference image to the image dynamic range. The intrusion size is kept at a constant fraction of line width, close to the printability threshold for that defect type, which is independently derived using EUVL aerial image simulations. Furthermore, the polarization state of the illuminating light is varied among realizable choices of optical configuration, labeled A, B, and C.

Figure 8. Dependence of defect contrast on Half-Pitch (wafer scale) for 2D Intrusion defects in 1:1 L/S pattern, for conventional imaging (upper row), and off-axis imaging (lower row) configurations, and three states of polarization of the illumination (columns).
The effects of illumination and polarization modes on defect contrast are significant. For this inspection performance metric, as well as the pattern contrast case, the ARC-based designs persistently show less performance than the alternatives. We also find that the bare TaN design maintains performance close to the booster design, raising the possibility that an absorber design without a cap layer to modify 193nm reflectance may provide an acceptable inspection solution.

4.3 Summary of Simulation results for 1D geometry

Figure 9 summarizes a large number of simulations of inspection performance by displaying the “scorecard” of the relative performance of three absorber designs for multiple defect classes in 1D pattern geometry, and for a variety of illumination conditions. Color coding reflects the inspection performance simultaneously through a range of half-pitch (wafer scale) values greater than 20 nm, with green indicating acceptable values of the performance metric for all pitch values.

Under off-axis illumination conditions, we find two absorber designs, combined with two polarization modes, which offer promising inspection performance for HP designs approaching 20 nm. It is especially encouraging to find multiple options available considering only 1D patterns and associated defects, since this will increase the probability of success in finding a manufacturable mask absorber design with acceptable EUVL process window as the set of layer and defect requirements widens.

5. EXPERIMENTAL INSPECTION RESULTS

5.1 Inspection performance using 193nm on a 32nm HP EUV mask

In collaboration with IMEC\(^6\), we obtained a programmed defect test mask, code-named DEF32. This mask featured 1:1 L/S geometry at 32nm HP (wafer scale), with a series of defect types and sizes. Wafers were printed using an ADT scanner. SEM review was used on printed wafers to verify defect printing status. Inspection was performed on a Teron
610, using 55nm pixel size in reflected light mode, corresponding to conventional imaging configuration. Multiple inspection passes were used to estimate capture rate performance as a function of nominal defect size.

Figure 10 compares the capture rate results with the SEM review results. Inspection on Teron 610 captured nearly all of the programmed defects on the 32nm HP mask. Rows 3, 5 and 6 show 100% capture of programmed defects in all 9 defective die. Comparing SEM review with inspection results, we find that inspection on the 610 captured 100% of the printing defects for these test patterns.

![Figure 10](image)

- Mask capture rates are from three scans of each defect on each die

Figure 10. Summary of inspection and review results for a 32nm HP (wafer scale) programmed defect test mask. Upper box shows EUVL printing status for defects ranging from large (left, 1) to small (right, 13). Lower box shows Teron 610 inspection capture rate (CR) results for the same defects.

6. EUVL MASK INSPECTION ROADMAP

Timely supply by equipment companies of capability for EUV mask inspection and metrology systems is a concern to the semiconductor industry. To avoid delays to the successful insertion and ramp of EUV Lithography, Sematech has formed a consortium to focus attention and stimulate investment in mask tool development. In the area of patterned mask inspection, a key consideration for decisions about the pace of new system development is the performance and extendibility of current or near-term optical inspection solutions, such as Teron. On the strength of our simulation results, a sample of which has been reviewed in this report, as well as the experimental tests underway, we expect the Teron platform to meet industry requirements for pattern inspection of EUVL masks deep into the 2X nm HP node.

Patterned mask inspection tools can be usefully applied to EUVL masks in three areas: blank shops, mask shops, and wafer fab requalification. In a paper at the SPIE 2010 Advanced Lithography conference, we present experimental results for Teron as applied to EUV blank mask inspection, demonstrating performance on blank phase defects adequate for 32nm HP requirements, and indicating a path to meet 22nm HP requirements. Future publications will address application of Teron to mask requalification inspections in the wafer manufacturing environment.

7. CONCLUSION

Experimental results for Teron inspection of current patterned EUVL masks, as well as rigorous simulation-based estimation of inspection capability for future 2Xnm HP designs, indicate that the Teron platform will support semiconductor industry needs for pattern mask inspection well into the 2Xnm HP node. Through ongoing collaborations
with leading mask shops to fabricate programmed defect test masks for the leading material candidates, we plan to secure experimental confirmation of capability for the 2X nm HP node. In addition to filling pattern inspection tool requirements, gaps arising in blank inspection tool capability can be filled by Teron, mitigating risk that blank defectivity reduction will be inhibited by inadequate inspection capability.

REFERENCES

[6] DEF32 EUV mask supplied courtesy of Rik Jonckheere, IMEC.