Visualizing the Wafer’s Edge

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Silicon wafers have edges, where the wafer ends and something else — a wafer stage, a chuck, or a robot arm — begins. Within this critical edge zone, thermal cycling and plasma exposure can degrade film adhesion, robots can break off particles from the edge bevel, and wet processes can cause delamination. Particles from all of these sources can contaminate devices across the wafer surface, or can migrate to the lithography tool’s exposure stage. New, high-productivity edge inspection technology allows chipmakers to find defect sites at the wafer edge and correlate them with yield results.

Process specifications have long recognized an edge exclusion zone, in which uniformity specifications are not necessarily met and process performance is not guaranteed. Die which encroach into the exclusion zone are not expected to function. Yet the existence of an edge exclusion zone implies that all other die on the wafer should be fine, whether they are near the edge or not. In reality, though, what happens on the edge can easily affect the rest of the wafer. The transition from a planar surface to the wafer bevel and apex regions creates a high-stress area susceptible to film delamination.

During process integration, interfacial stress may cause films to not adhere properly to the underlying layers in these regions. Wafer handling robots and other mechanical contact can chip films coating the edge bevel, breaking off particles. Thermal cycling and contamination sources can degrade film adhesion, causing blisters along the edge. If these blisters pop during handling, more particles result. Wet processes can erode edge films like waves attacking a coastline, causing delamination and generating more particles. Immersion lithography in particular drags a fluid bubble across the wafer at high speed, generating a virtual tsunami at the edge of the wafer. Particles from all of these sources can contaminate devices across the wafer surface, or can migrate to the lithography tool’s exposure stage. A benchmark study of ten fabs found that yield in the near-edge region was as much as 50% less than yield in the center region (Figure 1). More than half of near-edge yield loss was due to defects, rather than parametric variation.

Edge defectivity is not unique to 300mm wafers; the benchmark study found near-edge yield loss on both 200mm and 300mm wafers. However, the larger wafer size places more die near the edge. A 10mm-wide annulus at the edge of a 300mm wafer has an area of about 9110 mm², while one at the edge of a 200mm wafer has about two-thirds the area, encompassing about 5970 mm². In fact, the 10mm ring at the edge of the 300mm wafer accounts for about 13% of the total wafer area, and about 23% of the new area gained by the larger wafer size. Clearly, high yield loss in the near-edge region can have a significant impact on overall wafer yield and fab profit. In a typical situation, the edge zone might contain 150 die and suffer 30% excess yield loss. Valuing the lost dies at US $5.00 each and assuming 10,000 wafer starts per week, edge defects could be responsible for as much as US $2.5M in lost profit per week.
Defects are There, But How to Monitor Them?

Until recently, edge defect inspection focused on chips, cracks, and other kinds of structural damage to the wafer itself. Though catching these flaws at incoming inspection is important, structural damage is rare once wafers enter the production line. Process-induced edge defects often involve interactions among several process steps. For example, an area of poor adhesion might originate with a water spot or other residue, but the actual delamination might be caused by thermal expansion and contraction of the film during subsequent processing. Once a blister exists, further thermal expansion can allow it to grow, or mechanical contact can crush it. All of these effects are more commonly seen in the BEOL interconnect process, after several metal and dielectric layers have accumulated on the edge bevel.

For effective process control, fabs must both identify edge defects and sort them into the appropriate defect types. Both tasks are especially challenging because the edge region is very noisy. It may have varying thicknesses of several different films and contain numerous chips and scratches due to normal handling. While pre-production wafer inspection is likely to find only a handful of defects, applying the same techniques to a BEOL product wafer might find hundreds, or even thousands of abnormalities. SEM review is slow, can typically extend only up to the upper bevel region and large scale review is not economically feasible (Figure 2).

Some systems attempt to apply existing inspection technologies to edge defect detection. One approach relies on laser scattering, currently used for inspection of incoming wafers and unpatterned particle monitors. While the technology works well for these applications, the technology is not sensitive to most IC manufacturing defects related to films, such as delamination, flakes, and residues.

Brightfield and darkfield imaging are important tools for patterned wafer inspection and defect classification, and have also been applied to edge defect detection. Yet this technology also faces severe challenges. Patterned wafers have moderate topography, but the surface is still essentially planar. Depth-of-focus requirements are moderate, with no more than a few microns separating the tallest peaks from the deepest trenches. The edge region, in contrast, includes the full 3mm width of the edge exclusion zone. Defects can appear on the top surface of the wafer, the top bevel, the apex of the bevel, the bottom bevel, or the bottom surface of the wafer. A single CCD camera focused on the edge cannot hope to keep the entire region in focus at the resolution needed for micron-scale defect imaging (Figure 3). Without a clear image, accurate defect detection and classification is impossible. Another compromise to address the DOF challenge results in imaging at lower magnifications, resulting in a resolution compromise.

Because CCD imaging depends on what is essentially a microscope, with discrete optics and a limited field of view, designing a system that can image the whole near-edge region is difficult. The imaging camera itself is fixed in place, adding another requirement for multiple cameras for wider coverage – an option not practical for production-level monitoring.

Finally, defect imaging fidelity (color, shape, etc.) is impacted by the viewing angle (angle of incidence). Detection algorithms based on color and contrast have trouble separating actual defects from normal edge variations.
A New Approach

KLA-Tencor’s new edge inspection platform, utilizing optical surface analysis (OSA) technology, addresses these challenges with a revolutionary multi-sensor approach. This technology is already well established in the hard disk drive and compound semiconductor markets.

The tool works by imaging light emitted from the edge region (Figure 4). The laser source traces a beam of polarized light over the wafer edge – from top surface to bottom surface. Detectors capture both scattered and reflected light, measuring scattering intensity, polarization, beam deflection, and phase contrast. Each of the four resulting images supplies different information (Figure 5). The reflected light and phase channels are most sensitive to film defect sources, such as delamination, flakes, and residues. The scattered light channel is most sensitive to particle sources, chips, and cracks. Together, the images give a complete picture of the wafer edge.

Comparing different images from the same region can help differentiate between delamination, particles, and other defects. Though the imaging data is helpful in itself, automated defect detection and classification makes it even more useful, giving a defect map that is fully comparable to the maps provided by wafer die inspection tools. Process engineers can trace die loss to its source at the wafer edge in much the same way that they would attack any other yield problem.

Integral Part of a Complete Yield Solution

Wafer maps and full die inspection gave manufacturers the ability to see clusters of defects, separating random particles from defects clearly attributable to process problems. Partial die inspection has helped manufacturers track defects originating near the edge exclusion zone, warning of potential problems before they could spread to product die. Edge inspection completes the package, allowing manufacturers to find defect sites at the wafer edge itself and correlate them with yield results (Figure 6).

In order to recoup their investment in 300mm wafer manufacturing, fabs must maximize the yield from the “new” wafer area that the larger wafers provide. Much of that area lies near the wafer’s edge, in a region known to suffer from poor yield. Better detection and classification of edge defects is essential to overall wafer yield and, ultimately, fab productivity. The proven technology of KLA-Tencor’s edge inspection system supports rapid detection and accurate classification of these critical defects.

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