Etch Process Monitoring by Electron Beam Wafer Inspection

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Using E-beam inspection to establish defectivity levels from contact etch, Etch Process Window Qualification (Etch-PWQ) can provide accurate yield data to help users center the etch process within the process yield window, then monitor the etch process condition.

Process Window Qualification is a technique commonly used with optical and electron beam wafer inspection to keep the lithography process centered within the process window. Different dies across the wafer are exposed with varying focus and dose parameters. An inspection is used to determine the defectivity of the dies with different exposure conditions, and special software is used to analyze the results.

For etch processing, it is also critical to center the process within the process window. For instance, under-etch on a contact layer can result in blocked or resistive contacts, while over-etch can cause shorts between source, drain, and/or gate on the transistor. Traditionally, wafer splits are used to determine optimum etch process conditions. Two or more wafers are used, and each wafer is processed with a different etch condition. Optical or electron beam inspection can then be used to compare overall wafer defectivity. Electrical test at the end of processing can provide confirmation. However, this approach can have several drawbacks. For instance, uncontrolled variables can add uncertainty to the data, especially if the defect signature used to determine the optimum process setting is subtle. These variables can include changes in prior layer processes, changes in the lithography, changes in etch process (or tool/chamber), and the stability variance in the inspection tool. For electron beam inspection, differences in the residual surface charge or atmospheric molecular contamination (AMC) between wafers can also affect the inspection results.

For these reasons, it would be preferred to use a single wafer in order to determine the optimum etch process condition. In this study, we have developed such a technique, and have successfully used it to optimize etch process conditions.

**Experimental Approach**

Three full-flow DRAM wafers with 0.11µm design rule were used in this study. All wafers were processed normally up to the contact etch step. On each wafer at the transistor contact etch level, various dies received either nominal etch process condition or one of several different etch conditions, as shown in Table 1. The dies were arranged to facilitate die-to-die comparison of nominal and test dies in an automatic wafer inspection tool. Columns of test dies were alternated with two

<table>
<thead>
<tr>
<th>Etch condition</th>
<th>Gas flow</th>
<th>Over-etch time</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nominal</td>
<td>20 sccm</td>
<td>69 seconds</td>
</tr>
<tr>
<td>Test 1</td>
<td>21 sccm</td>
<td>55 seconds</td>
</tr>
<tr>
<td>Test 2</td>
<td>19 sccm</td>
<td>69 seconds</td>
</tr>
<tr>
<td>Test 3</td>
<td>19 sccm</td>
<td>75 seconds</td>
</tr>
</tbody>
</table>

Table 1: Summary of the etch process conditions used for different die on each wafer.
columns of dies processed using the nominal condition. In this way, each test die could be compared to two adjacent nominal dies. In addition, the various test dies were distributed across the wafer so that the process signature could be distinguished from any wafer level signature that might be present. The wafer layout of nominal and test dies is shown in Figure 1.

In order to process the various etch conditions on different dies on a single wafer, multiple lithography steps were utilized. First the nominal dies were exposed and etched, while the test dies were protected by blank resist. Then the lithography and etch process steps were repeated for each of the different etch process conditions on the test dies, while the nominal dies were protected by unexposed resist. In this way, the various process conditions were all placed on a single wafer. Figure 2 shows a flow chart of the lithography and etch processing steps.

Following the etch process steps, wafer #1 was checked for contact size using a CD-SEM, then continued with normal processing through electrical test. Wafer #2 was removed from the process flow and inspected first with an eS31 electron beam inspection tool, then with an eS32 electron beam inspection tool. Wafer #3 was held after the contact etch step for potential further study, such as FIB or TEM.

Results
Initially wafer #2 was inspected on an eS31 electron beam inspection tool using a landing energy of 1000eV, beam current of 212nA, and a pixel size of 100nm. Field conditions were set up such that underetched contacts would appear brighter than normal contacts, which are dark. The inspection failed to show any significant correlation between the etch conditions and the die defectivity. However, end-of-line bit failure testing on wafer #1, which continued with normal processing, showed a definite yield loss correlated with the etch process conditions. The bit yield map is shown in Figure 3; slashes indicate dies with poor bit yield results.

At this point, the wafer was re inspected using an eS32, which has improved sensitivity and a wider range of optics settings. The inspection care area was extended to the very edge of the array, where it was found that most defects were occurring.
A special precharge step was implemented to bring the wafer surface voltage to a condition that enhanced the contrast of the defective contacts. Finally, the inspection pixel size was reduced to 70nm in order to further increase sensitivity. This time, subtle under-etch defects were detected that also correlated with both the etch condition and the end-of-line bit yield results. The defect map is shown in Figure 4. A good correlation was found between inspection defect density on wafer #2 and electrical bit yield on wafer #1. A review image from the inspection tool containing some defective contacts is shown in Figure 5.

ePM is a new eS32 algorithm currently under development at KLA-Tencor that can be used to find out-of-tolerance wafers more quickly than standard e-beam inspection. Images are taken from identical locations on each of a selected number (or all) dies on the wafer. The average gray level of each image, which correlates to the average secondary electron yield, is computed and mapped. Because slight process variations can cause a significant variation in secondary yield, this technique can be used to establish process tolerance limits on etch or other process steps. Figure 6 shows the ePM gray level map of the wafer, clearly indicating differences between nominal and test die. Figure 7 shows a comparison between the contact CD measured on wafer #1 and the average gray level seen by ePM, for each of the four etch process conditions. Again, there is excellent correlation between the two measurements. As expected, underetch conditions resulted in a brighter average gray level because the normal contacts are darker than the surrounding oxide.

**Conclusion**

Etch Process Window Qualification (Etch-PWQ) has been shown to be a promising technique for establishing defectivity levels from contact etch and for providing accurate yield data to center the etch process within the process yield window. By placing the experimental design on a single wafer, data uncertainty caused by wafer process variations or inspection tool drift is avoided. In order to see subtle under-etch defects from marginal etch process conditions, it was necessary to use a precharge step and to select optics conditions to optimize sensitivity. Good correlation was seen between the inspection defectivity and the electrical bit yield. Finally, ePM, an electrical process monitor capability on the eS32 inspection tool that measures secondary yield across the wafer, shows promise as a tool for monitoring the etch process condition.

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