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Advanced Patterning Technologies and the Role of Process Control

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In order to overcome the resolution barrier of 193nm immersion lithography at the 28nm design node, it became necessary for IC manufacturers to develop new patterning techniques, including double patterning and spacer pitch splitting. With the move to sub-10nm design nodes, the utilization of multi-patterning techniques has intensified, with triple patterning (LELELE), self-aligned quadruple patterning (SAQP), and other complex patterning technologies being utilized to achieve smaller design nodes. Multi-patterning has enabled continued shrinking of device features in the absence of the availability of EUV lithography. Fortunately, significant progress has been reported with EUVL[1,2]. While many challenges still need to be addressed – line edge roughness, pellicle technology, etc. – EUVL is reportedly on track for introduction at the 7nm design node with wider adoption for high volume manufacturing at the 5nm node. At these design nodes, the goal of EUVL will be to reduce the number of process steps required to form a single pattern. However, it is believed that multi-patterning techniques will still be necessary with EUVL to achieve production of the most advanced IC devices.

IC manufacturers face many technical challenges when implementing advanced multi-patterning, including: the proliferation of process and design systematic defects; extremely tight patterning specifications; and, the erosion of process margins. Both design and process engineers must be able to find and assess hotspots – critical die locations susceptible to design- or process-related systematic defects – in order to drive improvements that ensure the device design and fabrication techniques are stable for production. At the sub-10nm design nodes, the maximum error for patterning is ≤2.5nm for overlay and ~0.7nm for critical dimension uniformity (CDU) (table 1). Adding to the challenge of achieving these tight patterning specifications is that CD, overlay errors and defects are now convolved: overlay errors may appear as CD variations; CD variations may appear as bridging defects, etc. An error in the final pattern could have arisen from any one or a combination of these three sources. Moreover, since multi-patterning requires more process steps – such as deposition, etch, and CMP – to form a single pattern, the number of process layers that could cause or contribute to patterning errors has greatly increased (figure 1).

Technology Node	28	20	14	10	7	5
Overlay	9nm	6nm	4nm	3nm	2.5nm	1.5nm
CDU	4.5nm	3nm	2nm	1nm	0.7nm	0.5nm

Table 1. Maximum error budget for overlay and critical dimension uniformity (CDU) by design node.

In this environment, it has become necessary for IC manufacturers to: (1) utilize comprehensive strategies to find hotspots and patterning errors; and, (2) control process and patterning variations at the source.

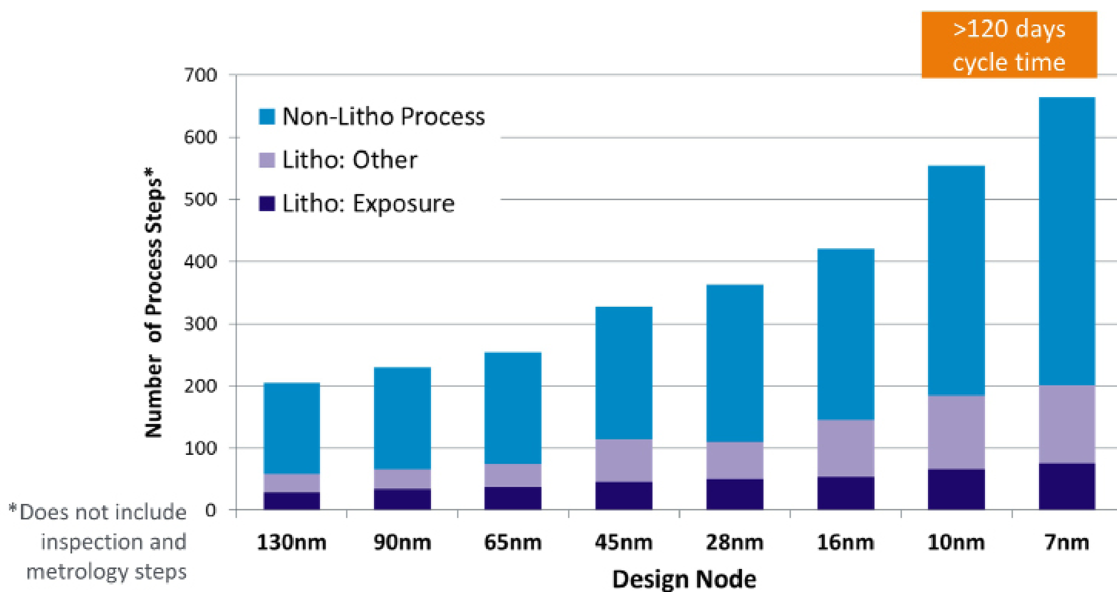

Figure 1. The number of process steps has increased dramatically at smaller design nodes due to the implementation of multi-patterning technologies[3]. These additional process layers increase IC manufacturing risk – each layer is a source of error and could affect final yield[4].

Figure 2 illustrates why a multi-faceted approach is required for finding and controlling patterning and process errors. For example, the source of overlay error is no longer simply scanner errors – overlay error can be correlated to fab-wide processes that affect parameters such as wafer shape, film thickness or temperature profile[5]. Therefore, it becomes critical to implement a process control strategy that identifies all sources of overlay variation – for example, measuring wafer shape after CMP, optimizing process tool/chamber temperature profiles, monitoring film thickness variations – in addition to measuring post-litho overlay error. Moreover, correcting variations at the source (i.e., optimizing the CMP process to eliminate wafer shape variations) helps fab engineers achieve optimal patterning.

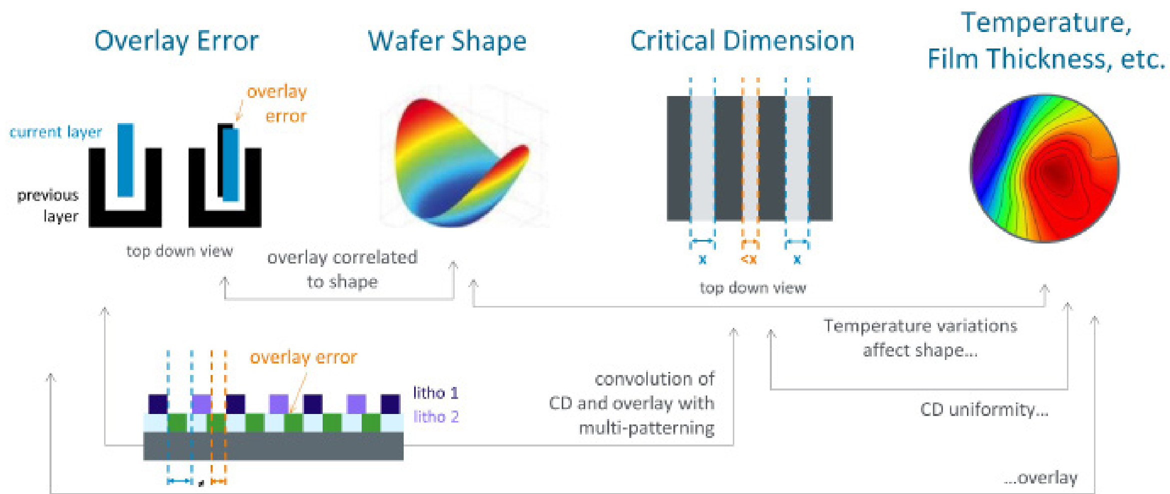

Figure 2. The source of overlay error is no longer dominated by scanner errors – overlay error can be correlated to fab-wide processes that affect parameters such as wafer shape, film thickness, CD or temperature profile.

With today's complex multi-patterning strategies, implementing a comprehensive process control strategy that utilizes fab-wide inspection and metrology systems with intelligent data analytics and process control loops can help fab engineers expediently identify and solve patterning issues.

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