ym/s Magazine

Process Watch: Salami Slicing Your Yield

By David W. Price and Douglas G. Sutherland

Author's Note: The Process Watch series explores key concepts about process control—defect inspection and metrology—for the semiconductor industry. Following the previous installments, which examined the 10 fundamental truths of process control, this new series of articles highlights additional trends in process control, including successful implementation strategies and the benefits for IC manufacturing.

Introduction

In a previous Process Watch article [1], we showed that big excursions are usually easy to detect but finding small excursions requires a combination of high capture rate and low noise. We also made the point that, in our experience, it's usually the smaller excursions which end up costing the fab more in lost product. Catastrophic excursions have a large initial impact but are almost always detected quickly. By contrast, smaller "micro-excursions" sometimes last for weeks, exposing hundreds or thousands of lots to suppressed yield.

Figure 1 shows an example of a micro-excursion. For reference, the top chart depicts what is actually happening in the fab with an excursion occurring at lot number 300. The middle chart shows the same excursion through the eyes of an effective inspection strategy; while there is some noise due to sampling and imperfect capture rate, it is generally possible to identify the excursion within a few lots. The bottom chart shows how this excursion would look if the fab employed a compromised inspection strategy—low capture rate, high capture rate variability, or a large number of defects that are not of interest; in this case, dozens of lots are exposed before the fab engineer can identify the excursion with enough confidence to take corrective action.

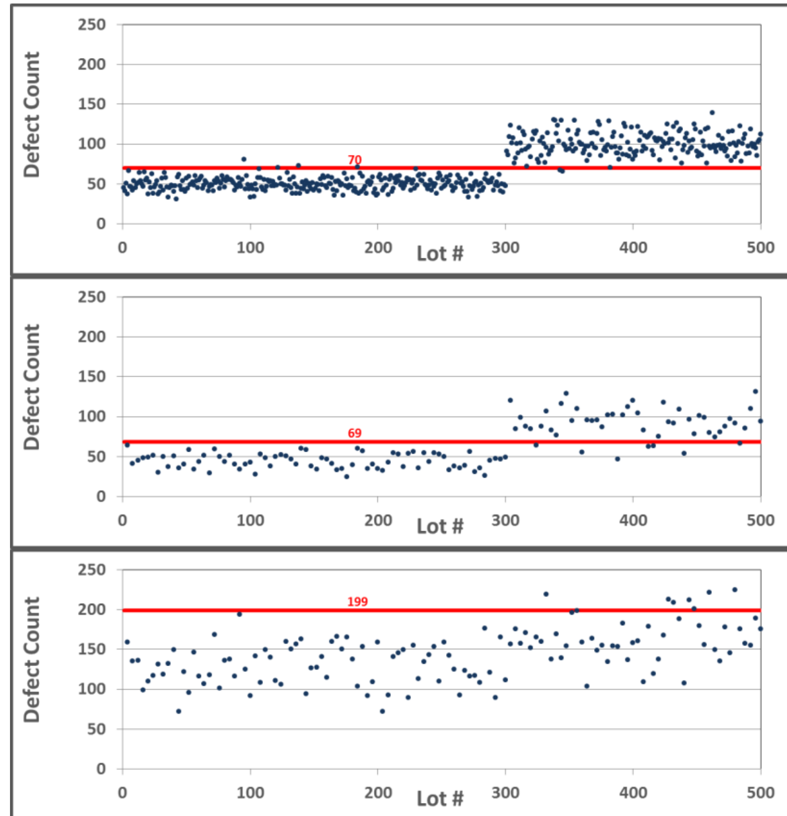

Figure 1. Illustration of a micro-excursion. Top: what is actually happening in the fab. Middle: the excursion through the lens of an effective control strategy (average 2.5 exposed lots). Bottom: the excursion from the perspective of a compromised inspection strategy (~40 exposed lots).

Unfortunately, the scenario depicted in the bottom of Figure 1 is all too common. Seemingly innocuous cost-saving tactics such as reduced sampling or using a less sensitive inspector can quickly render a control strategy to be ineffective [2]. Moreover, the fab may gain a false sense of security that the layer is being effectively monitored by virtue of its ability to find the larger excursions.

Micro-Excursions

Table 1 illustrates the difference between catastrophic and micro-excursions. As the name implies, micro-excursions are *subtle* shifts away from the baseline. Of course, excursions may also take the form of anything in between these two.

Table 1: Catastrophic vs. Micro-Excursions

	Catastrophic Excursion	Micro-Excursion
Wafer Level Yield Loss	High	Low
Baseline Shift	>>3x	< 3x
Frequency of Occurrence	Rare	Very Frequent
Onset	Step	Step or Drift
Ease of Detection	Usually Easy	Very Difficult
Typical Duration Before Detection	Short	Long

Such baseline shifts happen to most, if not all, process tools—after all, that's why fabs employ rigorous preventative maintenance (PM) schedules. But PM's are expensive (parts, labor, lost production time), therefore fabs tend to put them off as long as possible.

Because the individual micro-excursions are so small, they are difficult observe from end-of-line (EOL) yield data. They are frequently only seen in EOL yield data through the cumulative impact of dozens of micro-excursions occurring simultaneously; even then it more often appears to be baseline yield loss. As a result, fab engineers sometimes use the terms "salami slicing" or "penny shaving" since these phrases describe how a series of many small actions can, as an accumulated whole, produce a large result [3].

Micro-excursions are typically brought to an end because: (a) a fab detects them and puts the tool responsible for the excursion down; or, (b) the fab gets lucky and a regular PM resolves the problem and restores the tool to its baseline. In the latter case, the fab may never know there was a problem.

The Superposition of Multiple Simultaneous Micro-Excursions

To understand the combined impact of these multiple micro-excursions, it is important to recognize:

1. Micro-excursions on different layers (different process tools) will come and go at different times
2. Micro-excursions have different magnitudes in defectivity or baseline shift
3. Micro-excursions have different durations

In other words, each micro-excursion has a characteristic phase, amplitude and wavelength. Indeed, it is helpful to imagine individual micro-excursions as wave forms which combine to create a cumulative wave form. Mathematically, we can apply the Principle of Superposition [4] to model the resulting impact on yield from the contributing micro-excursions.

Figure 2 illustrates the cumulative effect of one, five, and 10 micro-excursions happening simultaneously in a 1,000 step semiconductor process. In this case, we are assuming a baseline yield of 90 percent, that each micro-excursion has a magnitude of 2 percent baseline yield loss, and that they are detected on the 10th lot after it starts. As expected, the impact of a single micro-excursion is negligible but the combined impact is large.

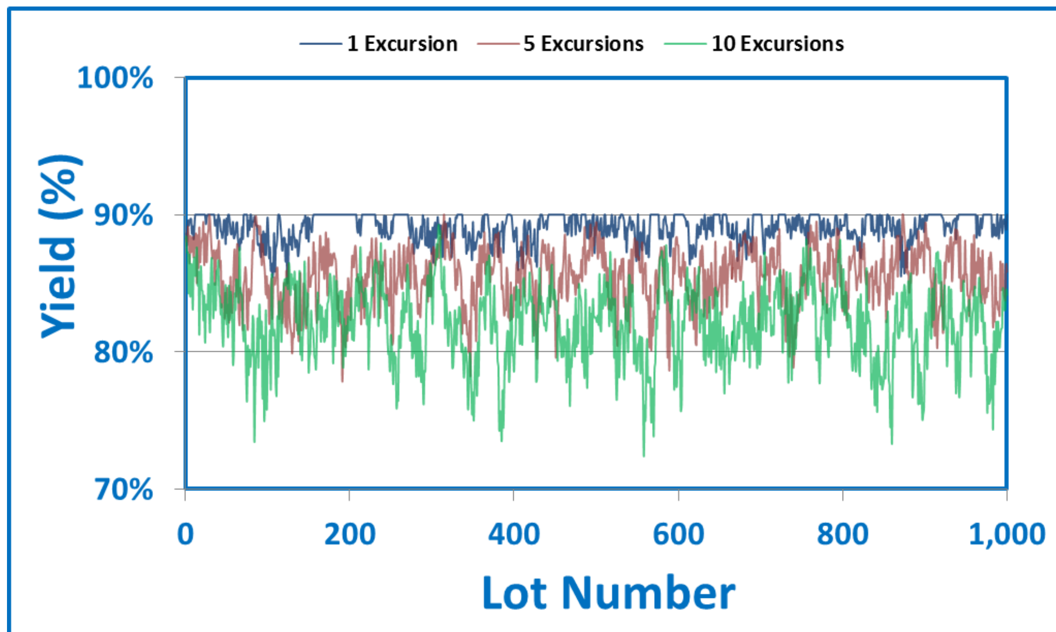

Figure 2. The cumulative impact of one, five, and 10 simultaneous micro-excursions happening in a 1,000 step process: increased yield loss and yield variation.

It is interesting to note that the bottom curve in Figure 2 would seem to suggest that the fab is suffering from a baseline yield problem. However, what appears to be 80 percent baseline yield is actually 90 percent baseline yield with multiple simultaneous micro-excursions, which brings the average yield down to 80 percent. This distinction is important since it points to different approaches in how the fab might go about improving the average yield. A true baseline yield problem would suggest that the fab devote resources to run experiments to evaluate potential process improvements (design of experiments (DOEs), split lot experiments, failure analysis, etc.). These activities would ultimately prove frustrating as the engineers would be trying to pinpoint a dozen constantly-changing sources of yield loss.

The fab engineer who correctly surmises that this yield loss is, in fact, driven by micro-excursions would instead focus on implementing tighter process tool monitoring strategies. Specifically, they would examine the sensitivity and frequency of process tool monitor inspections; depending on the process tool, these monitors could be bare wafer inspectors on blanket wafers and/or laser scanning inspectors

on product wafers. The goal is to ensure these inspections provide timely detection of small micro-excursions, not just the big excursions.

The impact of an improved process tool monitoring strategy can be seen in Figure 3. By improving the capture rate (sensitivity), reducing the number of non-critical defects (by doing pre/post inspections or using an effective binning routine), and reducing other sources of noise, the fab can bring the exposed product down from 40 lots to 2.5 lots. This, in turn, significantly reduces the yield loss and yield variation.

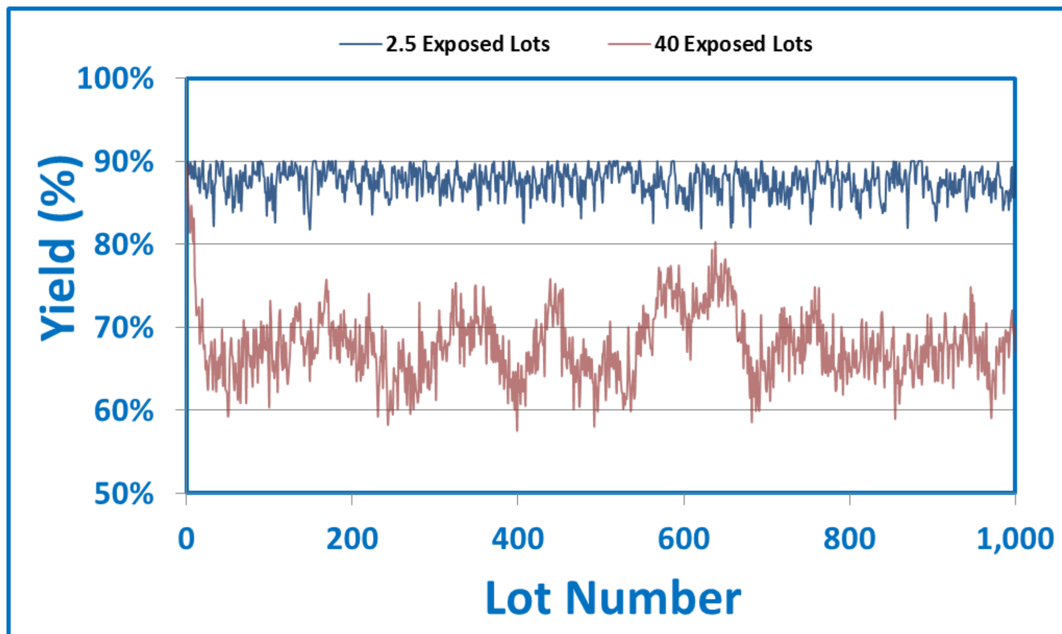

Figure 3. The impact of 10 simultaneous micro-excursions for the fab with a compromised inspection strategy (brown curve, ~40 lots at risk), and a fab with an effective process tool monitoring strategy (blue curve, ~2.5 lots at risk).

Summary

Most fabs do a good job of finding the catastrophic defect excursions. Micro-excursions are much more common and much harder to detect. There are usually very small excursions happening simultaneously at many different layers that go completely undetected. The superposition of these micro-excursions leads to unexplained yield loss and unexplained yield variation.

As a yield engineer, you must be wary of this. An inspection strategy that guards only against catastrophic excursions can create the false sense of security that the layer is being effectively

monitored—when in reality you are missing many of these smaller events that chip away or “salami slice” your yield.

References:

1) Process Watch: Know Your Enemy, *Solid State Technology*, March 2015
2) Process Watch: Fab Managers Don’t Like Surprises, *Solid State Technology*, December 2014
3) https://en.wikipedia.org/wiki/Salami_slicing
4) https://en.wikipedia.org/wiki/Superposition_principle

***About the Authors*:**

Dr. David W. Price is a Senior Director at KLA-Tencor Corp. Dr. Douglas Sutherland is a Principal Scientist at KLA-Tencor Corp. Over the last 10 years, Dr. Price and Dr. Sutherland have worked directly with more than 50 semiconductor IC manufacturers to help them optimize their overall inspection strategy to achieve the lowest total cost. This series of articles attempts to summarize some of the universal lessons they have observed through these engagements.