Process Watch: Yield Management Turns Green

By David W. Price, Douglas G. Sutherland and Kara L. Sherman

Author's Note: The Process Watch series explores key concepts about process control—defect inspection and metrology—for the semiconductor industry. Following the previous installments, which explored the 10 fundamental truths of process control, this new series of articles highlights additional trends in process control, including successful implementation strategies and the benefits for IC manufacturing. For this article, we are pleased to include insights from our guest author, Kara Sherman.

As we celebrate Earth Day 2018, we commend the efforts of companies who have found ways to reduce their environmental impact. In the semiconductor industry, fabs have been building Leadership in Energy and Environmental Design (LEED)-certified buildings [1] as part of new fab construction and are working with suppliers to directly reduce the resources used in fabs on a daily basis.

As IC manufacturers look for more creative ways to reduce environmental impact, they are turning to advanced process control solutions to reduce scrap and rework, thereby reducing fab resource consumption. Specifically, fabs are upgrading process control solutions to be more capable and adding additional process control steps; both actions reduce scrap and net resource consumption per good die out (figure 1).

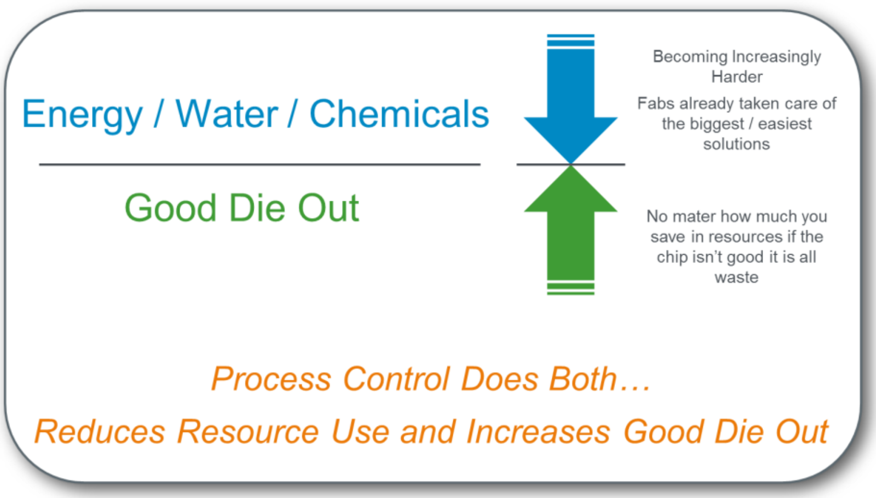

Figure 1. *The basic equation for improving a fab's environmental performance includes reducing resource use and increasing yield. Capable process control solutions help fabs do both by identifying process issues early thereby reducing scrap and rework.*

Improved Process Control Performance

Process control is used to identify manufacturing excursions, providing the data necessary for IC engineers to make production wafer dispositioning decisions and to take the corrective actions required to fix process issues.

For example, if after-develop inspection (ADI) data indicate a high number of bridging defects on patterned wafers following a lithography patterning step, the lithography engineer can take several corrective actions. In addition to sending the affected wafers back through the litho cell for rework, the engineer will stop production through the litho cell to fix the underlying process issue causing the yield-critical bridging defects. This quick corrective action limits the amount of material impacted and potentially scrapped.

To be effective, however, the quality of the process control measurement is critical. If an inspection or metrology tool has a lower capture rate or higher total measurement uncertainty (TMU), it can erroneously flag an excursion (false alarm), sending wafers for unnecessary rework, causing additional consumption of energy and chemicals and production of additional waste. Alternatively, if the measurement fails to identify a true process excursion, the yield of the product is negatively impacted and more dies are scrapped—again, resulting in less desirable environmental performance.

The example shown in figure 2 examines the environmental impact of the process control data produced by two different metrology tools in the lithography cell. By implementing a higher quality metrology tool, the quality of the process control data is improved and the lithography engineers are able to make better process decisions resulting in a 0.1 percent reduction in unnecessary rework in the litho cell. This reduced rework results in a savings of approximately 0.5 million kWh of power and 2.4 million liters of water for a 100k WSPM fab—and a proportional percentage reduction in the amount of resist and clean chemicals consumed.

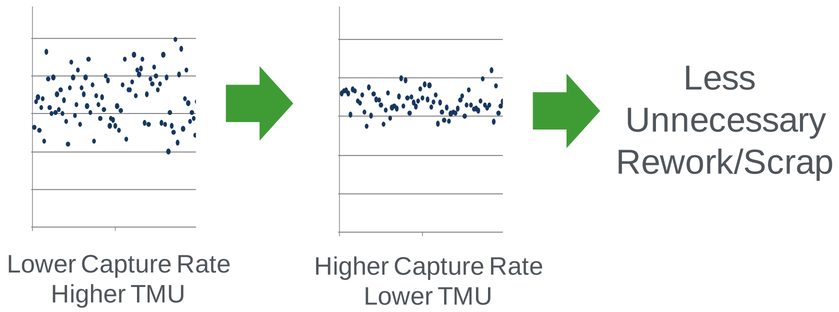

Figure 2. *Higher quality process control tools produce better process control data within the lithography cell, enabling a 0.1 percent reduction in unnecessary rework that results in better environmental performance.*

As a result of obtaining increased yield and reduced scrap, many fabs have upgraded the capability of their process control systems. To drive further improvements in environmental performance, fabs can benefit from utilizing the data generated by these capable process control systems in new ways.

Traditionally, the data generated by metrology systems have been utilized in feedback loops. For example, advanced overlay metrology systems identify patterning errors and feed information back to the lithography module and scanner to improve the patterning of future lots. These feedback loops have been developed and optimized for many design nodes. However, it can also be useful to feed forward (figure 3) the metrology data to one or more of the upcoming processing steps [2]. By adjusting the processing system to account for known variations of an upcoming lot, errors that could result in wafer scrap are reduced.

For example, patterned wafer geometry measurement systems can measure wafer shape after processes such as etch and CMP and the resulting data can be fed back to help improve these processes. But the resulting wafer shape data can also be fed forward to the scanner to improve patterning [3-5]. Likewise, reticle registration metrology data can be used to monitor the outgoing quality of reticles from the mask shop, but it can also be fed forward to the scanner to help reduce reticle-related sources of patterning errors. Utilizing an intelligent combination of feedforward and feedback control loops, in conjunction with fab-wide, comprehensive metrology measurements, can help fabs reduce variation and ultimately obtain better processing results, helping reduce rework and scrap.

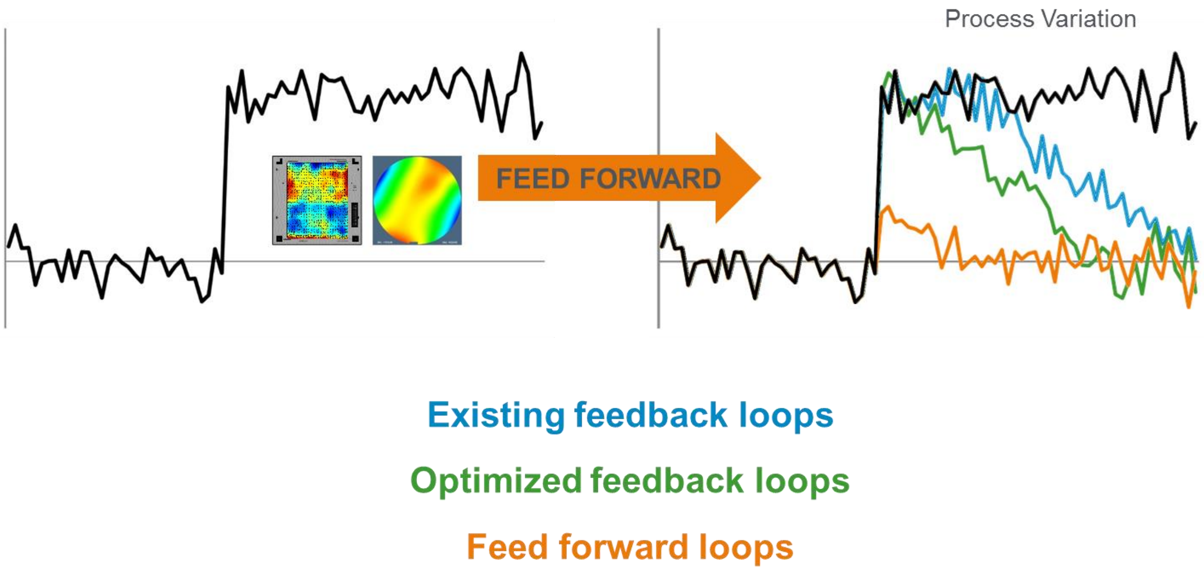

Figure 3. *Multiple data loops to help optimize fab-wide processes. Existing feedback loops (blue) have existed for several design nodes and detect and compensate for process variations. New, optimized feedback loops (green) provide earlier detection of process changes. Innovative feed forward loops (orange) utilize metrology systems to measure variations at the source, then feed that data forward to subsequent process steps.*

Earlier Excursion Detection Reduces Waste

Fabs are also reducing process excursions by adding process control steps. Figure 4 shows two examples of deploying an inspection tool in a production fab. In the first case (left), inspection points are set such that a lot is inspected at the beginning and end of a module, with four process steps in between. If a process excursion that results in yield loss occurs immediately after the first inspection, the wafers will undergo multiple processing steps, and many lots will be mis-processed before the excursion is detected. In the second case (right), inspection points are set with just two process steps in between. The process excursion occurring after the first inspection point is detected two days sooner, resulting in much faster time-to-corrective action and significantly less yield loss and material wasted.

Furthermore, in Case 1, the process tools at four process steps must be taken off-line; in Case 2, only half as many process tools must be taken offline. This two-day delta in detection of a process excursion in a 100k WSPM fab with a 10 percent yield impact results in a savings of approximately 0.3 million kWh of power, 3.7K liters of water and 3500 kg of waste. While these environmental benefits were obtained by sampling more process steps, earlier excursion detection and improved environmental performance can also be obtained by sampling more sites on the wafer, sampling more wafers per lot, or sampling more lots. When a careful analysis of the risks and associated costs of yield loss is balanced with the costs of additional sampling, an optimal sampling strategy has been attained [6-7].

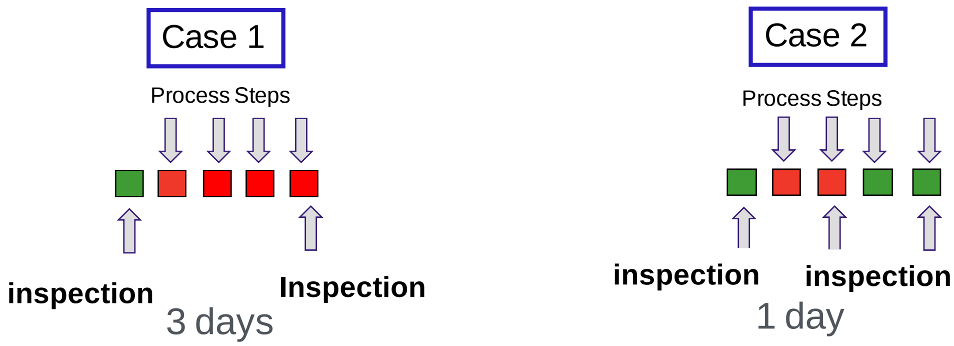

Figure 4. *Adding an additional inspection point to the line will reduce the material at risk should an excursion occur after the first process step.*

Conclusion

As semiconductor manufacturers focus more on their environmental performance, yield management serves as a critical tool to help reduce a fab's environmental impact. Fabs can obtain several environmental benefits by implementing higher quality process control tools, combinations of feedback and feedforward control loops, optimal process control sampling, and faster cycles of learning. A comprehensive process control solution not only helps IC manufacturers improve yield, but also reduces scrap and rework, reducing the fab's overall impact on the environment.

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Dr. David W. Price, Dr. Douglas Sutherland, and Ms. Kara L. Sherman are Senior Director, Principal Scientist, and Director, respectively, at KLA-Tencor Corp. Over the last 10 years, this team has worked directly with more than 50 semiconductor IC manufacturers to help them optimize their overall inspection strategy to achieve the lowest total cost. This series of articles attempts to summarize some of the universal lessons they have observed through these engagements.