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# EUV Lithography and Overlay Control

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One of the key parameters in IC fabrication is overlay – the accuracy of aligning pattern features to previously-patterned features (figure 1). The electrical contact between layers of a device – for example, from a transistor to a contact to an interconnect – depends on proper alignment of pattern layers. Minimizing overlay errors is important for achieving high yield and reliability, and for ensuring that devices meet performance specifications.

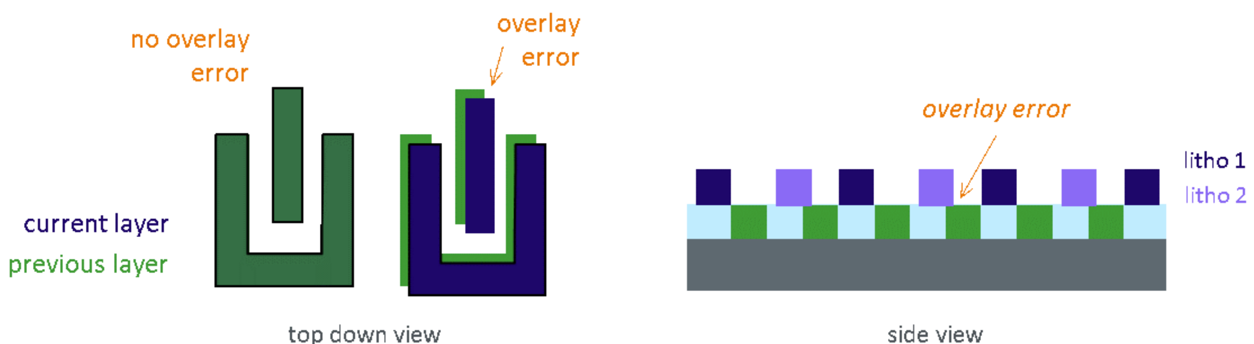



**Figure 1.** Overlay is the accuracy of aligning pattern features to previously-patterned features. Overlay error is a measure of the misalignment between two pattern features.

In order to achieve sub-20nm design nodes using 193i scanners, IC manufacturers have been using multi-patterning techniques, including both pitch splitting and spacer techniques. Pitch splitting includes double and triple patterning (for example, litho-etch-litho-etch (LELE)), while spacer includes self-aligned double and quadruple patterning (SADP, SAQP). These multi-patterning techniques greatly increase overlay complexity: in addition to achieving accurate inter-layer pattern alignment, it is also important to obtain accurate intra-layer pattern alignment (figure 2). In general, overlay control grows more complicated and the overlay error budget decreases as feature sizes become smaller and the number of mask layers associated with multi-patterning increases[1] (figure 3).

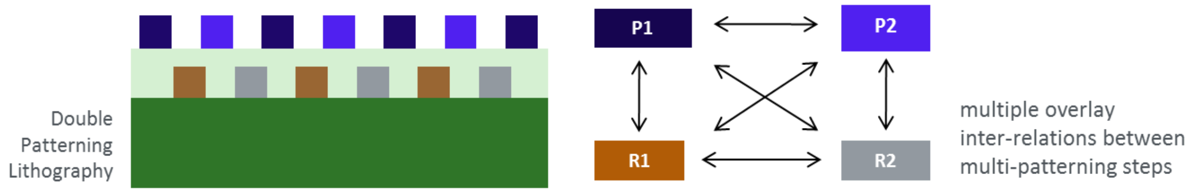
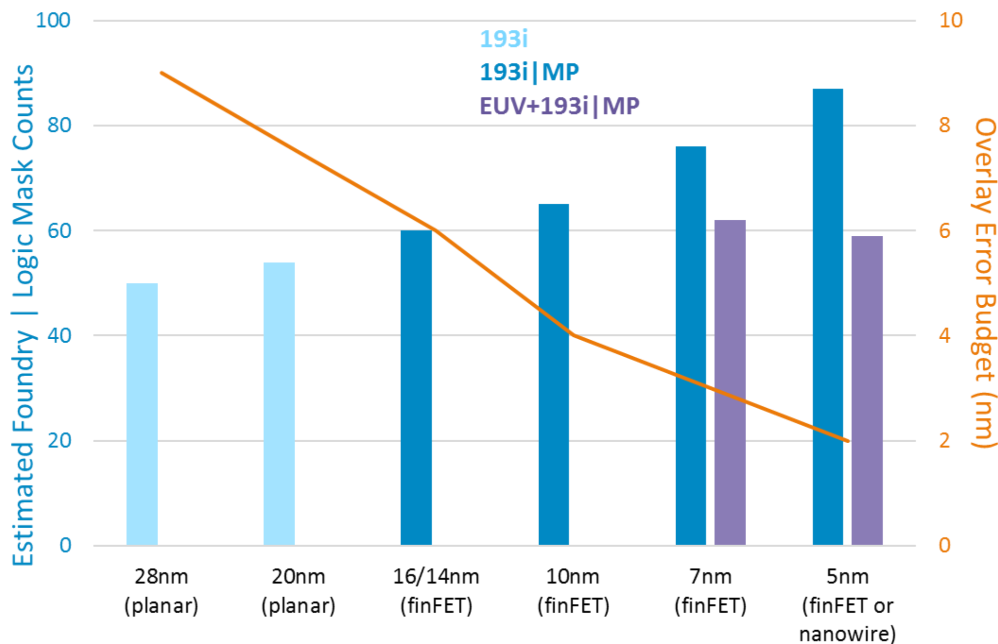



**Figure 2.** With multi-patterning schemes, overlay control becomes more complex. It is necessary to verify that pattern features have been correctly aligned to previously-patterned features, located on either the same layer or a prior process layer.

With the continued drive to shrink pattern dimensions, all major semiconductor manufacturers are actively engaged in furthering development of EUV lithography (EUVL) for production insertion in 2019-2020. The shorter wavelength of EUV scanners is critical for achieving smaller device pattern pitches. EUVL is also necessary for reducing process complexity at advanced design nodes[2], as it will allow fabs to use single-patterning for some layers that currently require multi-patterning techniques (figure 3). This reduces both the number of mask counts and overlay complexity[3]. While the industry has continued to make forward progress in readying EUVL for production, there are still many challenges that need to be addressed[4,5], including understanding how this lithography transition affects overlay. Below we outline some of the expected overlay challenges associated with the transition to EUVL.




*Source: KLA-Tencor; data shown assumes advanced SoC BEOL Mx layer counts, low-risk EUV implementation at 7nm, more aggressive EUV implementation at 5nm and 1D layout for all patterns.*



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**Figure 3.** Chart showing the estimated number of litho masks for shrinking design nodes (blue and purple bars) and the overlay error budget per design node (orange line). In moving to sub-20nm design nodes, IC manufacturers implemented multi-patterning (MP) techniques, resulting in an increase in the number of mask layers needed to produce a device, reduced overlay error budget and increased overlay control complexity. The introduction of EUVL at the 7nm and 5nm design nodes will allow use of single-patterning for several layers that currently require multi-patterning techniques. This will reduce the number of mask layers (purple bars) and overlay control complexity. However, the smaller design nodes will continue to drive down the maximum overlay error budget.

**Mix-and-Match Overlay.** For critical layers in current process flows using 193i lithography, pattern layers for a given wafer are printed using the same stage/chuck on the same scanner. The overlay performance achieved using this lithography strategy is called dedicated chuck overlay (DCO). Use of a dedicated scanner and chuck for lithography reduces inter-scanner and inter-chuck distortion effects, resulting in DCO overlay error <1nm. When EUVL is first implemented in production, it will be used for a few layers – likely, cut masks and contacts with eventual migration to metal 1 layers. All other layers will be patterned with 193i scanners[6]. This hybrid scanner operation eliminates any possibility of using a dedicated scanner and dedicated chuck to support tight overlay performance specifications. Instead, fabs will be forced to optimize mix-and-match overlay (MMO) – the overlay performance obtained using different scanners for printing different layers on a given wafer. With overlay specifications for advanced DRAM and logic at ~2.5nm, fabs will need to implement strict 193i-to-EUV scanner matching strategies or risk consuming 60-100% of the overlay budget on just MMO. In addition, fabs will need to implement dense in-field overlay measurements to monitor the MMO performance.

**Thermal Effects.** Within EUV scanners, stray light is a concern. In particular, stray infrared (IR) light may serve as a heating component during the exposure sequence of printing a wafer. When exposed to heat, silicon is slightly expansive, a property that could result in slight pattern variations that manifest as overlay errors. As development efforts with EUVL progress, it will be important to characterize overlay performance as a wafer is exposed. Do overlay error and the required overlay corrections vary during the exposure sequence? Do these thermal effects result in the need for an additional higher order field term for overlay corrections? While it's important to understand how thermal variations affect overlay, it will also be important to understand the fundamentals of thermal variations, lens heating impacts, etc., of the scanner during the exposure sequence – are they repeatable and can they be controlled?

**Focus Variation.** EUVL may create overlay issues that are related to focus control. EUVL has a much larger focus window than 193i, likely resulting in larger cross-wafer and cross-field focus variations. This may create non-linear overlay errors that require specific higher-order corrections for each exposure. There is also a loss of telecentricity with the mask in EUVL, which can cause the best focus for different features across a die to be slightly different. Additionally, EUVL mask backside particle defects, which will require reticle backside inspection for monitoring during production, can induce localized focus errors. These localized focus errors and variations can cause overlay issues. Overlay measurements are primarily performed on targets located in the scribe area of the die. So, the coupling of EUVL mask backside defects and telecentricity can result in differences in best focus for the target and device pattern. This will drive the need for innovations in overlay target design so that the designs correctly reflect device performance. Finally, there are several other characteristics of the EUV scanner that can create focus variations that result in overlay errors, including mask bending due to heating during exposure and thermal effects.

**Overlay Alignment Schemes.** One of the benefits of EUVL is that it reduces patterning complexity; pattern pitches that required multi-patterning techniques with 193i scanners can be produced in a single patterning step with EUV scanners. This results in much simpler pattern alignment schemes, fewer overlay steps and some loosening of overlay specifications. However, it is expected that overlay challenges will not become easier with EUVL. Instead, the challenges will shift: there may be fewer overlay steps, but this benefit will be offset by the higher sampling required due to intra-field effects caused by sources of variation such as thermal and focus variations.

**Stochastics.** Line edge roughness (LER) caused by stochastic noise is one of the top concerns for EUVL. High LER affects the accuracy of all measurements, including overlay error measurements. While LER affects all overlay measurement technologies, for SEM-based overlay measurements, high LER may require measurement of multiple edges for statistical validity, which will increase the needed overlay target size.

**Overlay Measurement Technology**. There are two primary measurement technologies used for overlay metrology – imaging and scatterometry. In general, scatterometry provides higher precision for overlay error measurements while imaging is less susceptible to process variations[7]. In the early development stages of any technology transition, including EUVL, there is much variation as processes are characterized and process flows are optimized. Thus, during development, imaging-based overlay measurements are often used. As EUVL moves from

development to ramp to production, and processes stabilize, overlay measurements may migrate to scatterometry to take advantage of the improved precision for high volume overlay control.

Another factor to consider is the effectiveness of current overlay metrology technologies for measurement on EUV resists, which are different materials and thinner stacks compared to 193i resists. The latest-generation imaging- and scatterometry-based overlay metrology systems include tremendous measurement flexibility, incorporating a range of wavelengths, polarizations and other innovations that enable measurement across a range of process layers and litho stacks. Early characterization of EUV layers using both imaging- and scatterometry-based overlay metrology systems has shown good performance, with no issues measuring on the thin EUV resist stacks.

**Summary.** The transition to EUV lithography removes some of the overlay complexity associated with 193i multi-patterning schemes, while it introduces new sources complexity: the need for mix-and-match overlay; thermal effects from stray light; focus variation from deviations in telecentricity in masks; line-edge roughness complications to edge determination; and the need to measure thin photoresist.

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