Editorial
"EUV is coming"

Moshe Preil, KLA-Tencor Corp.

After many years of hearing that EUV is almost ready for prime time, the tide is finally coming in. A decade of slow but steady progress has resulted in exposure tools that can expose on the order of 1,000 wafers a day on a regular basis. This may be shy of the requirements for high volume manufacturing (HVM), but it is certainly more than enough to support solid development programs and pilot line production. Almost all leading edge manufacturers have announced plans for early introduction in the 2018-19 timeframe, with HVM to follow within 1-2 years if the economics and technology are proven to be viable. Papers at the SPIE Photomask Technology (BACUS) + EUV Lithography conference in Monterey, SPIE Advanced Lithography 2017 conference and Photomask Japan 2017 symposium all highlighted the emerging maturity of EUV tools and processes, as well as the remaining challenges. It is certainly an exciting time for the EUV community, and a time of impending change for the mask making world.

From a mask making perspective, the key technical issues have long been identified as mask blank and multi-layer defectivity, mask blank and patterned mask inspection, defect review and pellicles. Mask blanks, tools and processes are now able to support the needs of development and pilot line volumes, and inspection of patterned masks is satisfactorily addressed today using a combination of DUV mask inspection and broadband plasma optical patterned wafer inspection focused on repeating defects on wafers. Wafer print verification helps to identify marginal patterns that are susceptible to stochastic failure ("soft" repeating defects).

There is reasonable optimism that with continued progress there should be no showstoppers to HVM introduction by the end of the decade. Even if actinic patterned inspection and aerial image review are not fully mature by then, e-beam based mask inspection can satisfy almost all requirements for pre-pellicle inspection, and there will be continued evolutionary progress to extend DUV mask inspection. Other areas of EUV mask inspection requiring greater attention are mask blank and backside defects. Since the reticle is electrostatically clamped to the chuck, micron size particles on the reticle backside can result in significant pattern placement errors which may vary as a function of feature geometry and orientation. Early detection of backside particles is critical to avoid contaminating the reticle chuck or otherwise introducing foreign particles into the reticle handling and storage system.

Significant progress towards developing pellicle solutions that can survive high power use in production and be integrated into the mask inspection and fab requalification cycle has been

reported. Other issues relating to mask infrastructure, such as multi-beam mask writers, computational lithography solutions for OPC including the added complexity of mask 3D effects and non-telecentric optics with a 6-degree chief ray angle, and clean tools for handling, cleaning and storage of EUV reticles, are all well on their way to HVM readiness.

But while the mask making world is well aware of these issues and progress towards solutions, gaps still remain in the complete integration of mask and wafer processing to meet the final requirements for product wafers. In order to fully understand the requirements imposed on the mask side of the industry, we must develop a comprehensive view of EUV manufacturing requirements as a whole. Mask solutions which are not fully integrated with wafer production requirements run the risk of creating serious capability gaps. In particular, the mask making world must comprehend the implications of stochastic variability during wafer exposure in order to ensure that the masks we make will print correctly in volume manufacturing.

The issue of stochastic variation was a major theme at the 2017 SPIE Photomask Technology (BACUS) + EUV Lithography conference. Despite all of the progress in EUV source power, the high throughput numbers being cited as targets for HVM introduction still require low dose resist exposures with associated penalties in line edge roughness (LER) and pattern placement roughness (PPR) caused by stochastic effects such as photon shot noise. Complete edge placement error (EPE) budgets must capture the contributions due to reticle LER and placement error, wafer process LER and PPR (including stochastic noise), and systematic terms such as pattern dependent focus and placement errors. With total EPE budgets in the low single nm range, it is increasingly difficult to allocate a specific number of nm to each term individually. Total EPE budgets will become the final metric of success or failure of the entire process. No part of the budget, whether mask or wafer related, can be fully specified independent of the other terms.

Stochastic effects also complicate metrology and inspection requirements. How small of a defect can be detected reliably or how accurately CD and placement errors can be measured is highly dependent on pattern roughness at both mask and wafer levels. Stochastic effects also create the possibility of a new class of defects known as soft repeaters, or more properly stochastic defects. Determining the printability of a suspect location on a mask may no longer be accomplished by simply exposing a wafer and seeing if the defect prints in every field; it is now important to see if the defect prints in even a small fraction of the fields. Detecting CD defects on a background pattern with 3-5 nm of LER will be challenging, to say the least. CD uniformity presents similar challenges. Recent papers at SPIE demonstrated how non-Gaussian tails on CD distributions require extensive analysis and consideration of up to 7 sigma of variation as opposed to the traditional 3 sigma values.

EUV is coming. The successful adoption of this technology for HVM may drive Moore's Law for another few nodes, but it will not be easy. The mask making community must play a key role in enabling viable EUV strategies for the entire process. Co-location of the

EUV Litho Symposium with the BACUS conference in Monterey was a solid step in driving critical interactions between the mask and wafer process worlds. As a community, we can all contribute to breaking down artificial barriers between mask and wafer “silos” and developing comprehensive solutions to enable EUV in production.

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