Device Overlay Method for High Volume Manufacturing

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ABSTRACT

Advancing technology nodes with smaller process margins require improved photolithography overlay control. Overlay control at develop inspection (DI) based on optical metrology targets is well established in semiconductor manufacturing. Advances in target design and metrology technology have enabled significant improvements in overlay precision and accuracy. One approach to represent in-die on-device as-etched overlay is to measure at final inspection (FI) with a scanning electron microscope (SEM). Disadvantages to this approach include inability to rework, limited layer coverage due to lack of transparency, and higher cost of ownership (CoO). A hybrid approach is investigated in this report whereby infrequent DI/FI bias is characterized and the results are used to compensate the frequent DI overlay results. The bias characterization is done on an infrequent basis, either based on time or triggered from change points. On a per-device and per-layer basis, the optical target overlay at DI is compared with SEM on-device overlay at FI. The bias characterization results are validated and tracked for use in compensating the DI APC controller. Results of the DI/FI bias characterization and sources of variation are presented, as well as the impact on the DI correctables feeding the APC system. Implementation details in a high volume manufacturing (HVM) wafer fab will be reviewed. Finally future directions of the investigation will be discussed.

Keywords: Overlay, overlay metrology, SEM overlay.

1. INTRODUCTION

Overlay has emerged as one of the most critical parameters in advanced semiconductor manufacturing. High volume manufacturing (HVM) process control is based primarily on optical metrology on specially designed targets, typically located in the scribe line area or in intra-die streets. Metrology is typically performed at develop inspection (DI), that is, after the litho step. Advantages of this scheme include high throughput metrology, layer transparency to optical metrology, and the ability to do rework. Figure 1a and 1b show typical examples of overlay metrology types. Scatterometry overlay (SCOL) and imaging overlay with advanced imaging metrology (AIM) marks. Due to the demands of excursion detection and advanced process control (APC), metrology at DI is done at a high frequency, typically every lot on all critical layers.

Much less frequently, overlay metrology is performed at final inspection (FI), that is after etch. FI overlay, though less common than DI, is typically done using scanning electron microscope (SEM) technology on the device structure rather

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than on specially designed metrology targets as shown in Figure 1c and 1d. Disadvantages of FI overlay using the SEM include low throughput and hence high cost, lack of transparency of some layers hence requiring decap process steps in some cases, and inability to rework out of spec material.

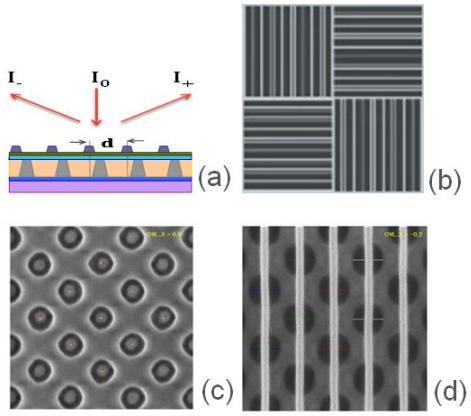

Figure 1: Overly metrology examples: (a) scatterometry overlay (SCOL) illustration, (b) Advanced Imaging Metrology (AIM) mark, (c) & (d) SEM on-device examples.

Moving to 1x DRAM processing requires an overlay spec of 2 nm in HVM. As is typical of advancing to new design nodes, new sources of variation must be addressed. Issues that may have been addressed manually or infrequently may require more frequent updates, more automation, and better analysis tools. The delta between DI overlay on metrology marks and FI overlay on device structures has required attention for many nodes. What is new is the relative size of this DI-FI bias, often significantly larger than the 2 nm OL spec on both the mask (or field) level and on the wafer level.

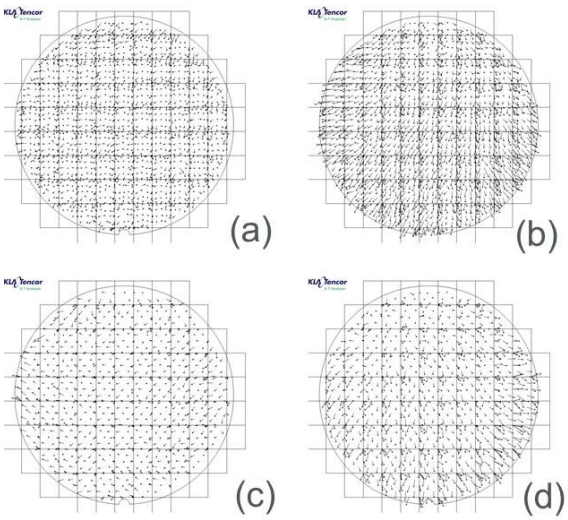

Figure 2: Wafer maps showing: (a) DI overlay with process corrections, (b) DI overlay without process corrections, (c) FI overlay, and (d) DI-FI bias.

Figure 2 shows an example of the DI-FI bias for DRAM "Layer A". Figure 2a shows the DI overlay with process corrections, 2b shows the DI overlay without process corrections. Both DI results are based on optical metrology on

scribeline metrology targets. Figure 2c shows FI overlay on device structures as measured by a SEM, and finally Figure 2d shows the DI-FI bias, that is the difference between DI overlay (without process corrections) and the FI overlay.

While there is significant opportunity for error and bias with SEM overlay metrology, for the purposes of this work, it is assumed that FI overlay as measured by the SEM is the overlay error that should be minimized for optimal device performance. The schema by which we minimize FI on-device overlay by targeting non-zero offsets at DI is called NZO or non-zero offsets. For improved process control required for the 1x nm DRAM node, the goal is to (1) characterize NZO, (2) minimize NZO, (3) minimize NZO variability, and (4) flag NZO excursions. To do this requires optimal target designs [1], optimized metrology recipes [2], the ability to track excursions, and a system to characterize and update NZO automatically. The focus of this work is automation and characterization of NZO for improved process control.

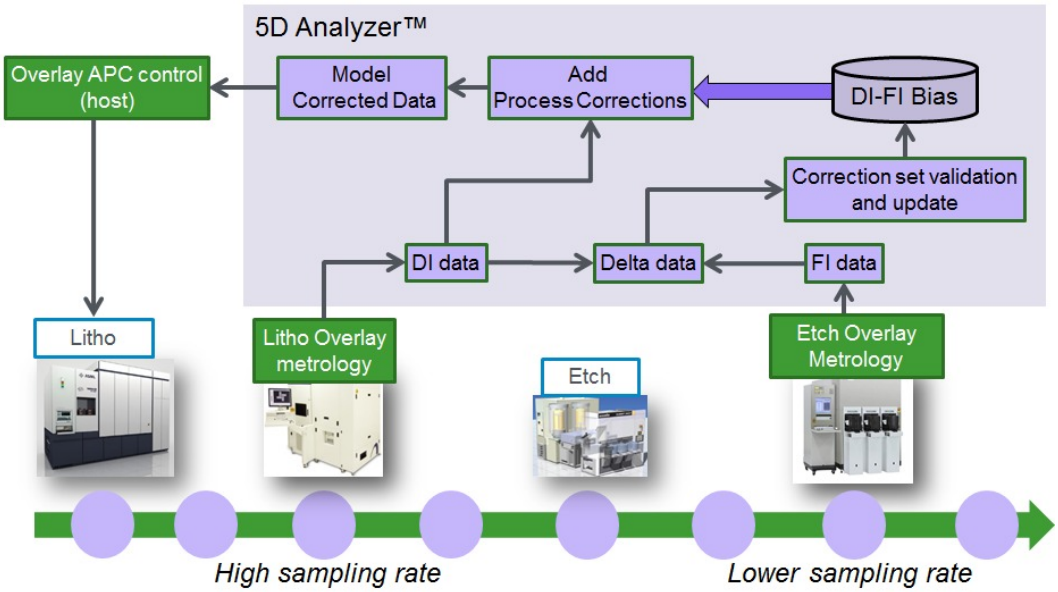

Figure 3: Schematic of automated process corrections update using KT Analyzer™.

Figure 3 shows a schematic of an NZO control scheme. The high frequency DI control loop based on optical after litho overlay is supplemented with a low frequency FI update after etch. Trigger points for FI updates can include process change points (e.g. process tool preventative maintenance or PMs), time based, or excursion based. Once triggered, the FI and DI data are subtracted to create a bias, which is then modeled and stored. The NZO bias is used to correct the DI process loop. In this way, the high frequency DI control loop effectively targets non-zero overlay in order that the FI overlay is minimized. As we drive to more advanced process nodes, the NZO process requires better automation, better analysis, and better process control.

In this study we looked at NZO for two DRAM layers. In one case we investigated lot-to-lot variation and the overlay budget breakdown using plan of record (POR) sampling. In the second experiment we looked at full map sampling on a single wafer.

2. LOT-TO-LOT BUDGET BREAKDOWN

The NZO control scheme described above requires relative stability of the DI-FI bias between updates. In our first study, we look at lot-to-lot variability in the DI-FI bias. In this example, we have single chuck data from 1 wafer each from 3 lots of layer A, and dual chuck data from 14 lots of layer B taken over a period of weeks. The sources-of-variation analysis involves modeling the wafers using a W3F3 model, that is a third order model across the field and across the wafer as is typical of an advanced control scheme. Figure 4 shows the sources-of-variation analysis for layer A and layer B. We show only X overlay in these examples, as that is the most critical axis for control. For layer A, we see the majority of variability is common across the lots during the time of the experiment. A small portion is variable from lot to lot. Finally, there is a portion of the variability that is not captured by the W3F3 model. The situation is similar for layer B, though the lot-to-lot variation and un-modeled portion comprise a larger percentage in this case.

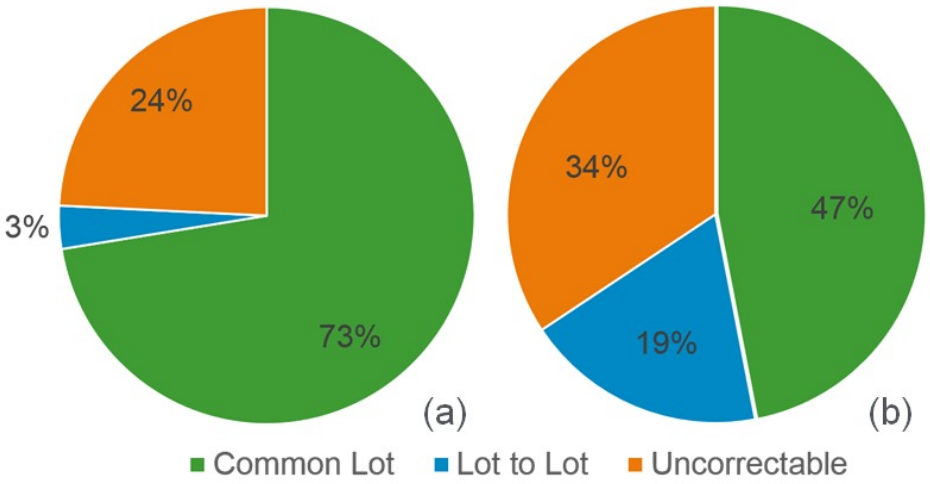

Figure 4: DI-FI bias sources of variation analysis for X overlay of (a) Layer A, and (b) Layer B.

Figure 5 shows an additional analysis of layer B, where 8 wafers are from chuck 1 and 6 wafers are from chuck 2. In this case we add the chuck-to-chuck component to the variability analysis. Not surprisingly, we see that the chuck-to-chuck variability is quite small, since the DI-FI bias is largely expected to be from non-litho origins such as etch or deposition.

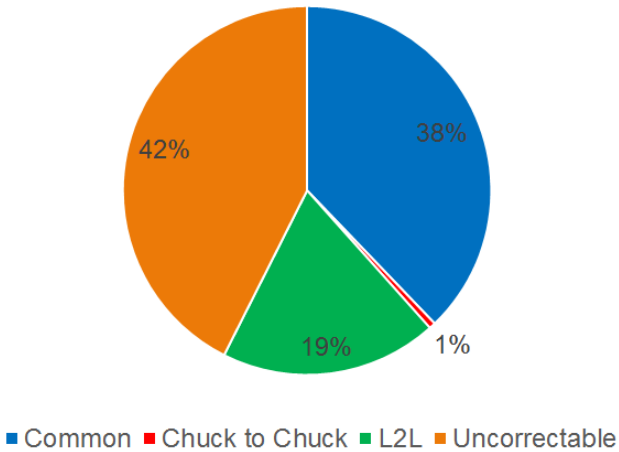

Figure 5: DI-FI bias sources of variation analysis for X overlay of Layer B including chuck-to-chuck.

3. FULL MAP ANALYSIS

In this second study, we analyze full map overlay data from a single wafer. Figure 6 shows the full map DI-FI bias un-modeled fingerprint. As can be seen the bias is generically in the form of an across wafer effect, rather than an across field effect, again not surprising since the origin of the bias is typically expected to come from outside litho. In this case we see variability approximating a wafer-scale signature.

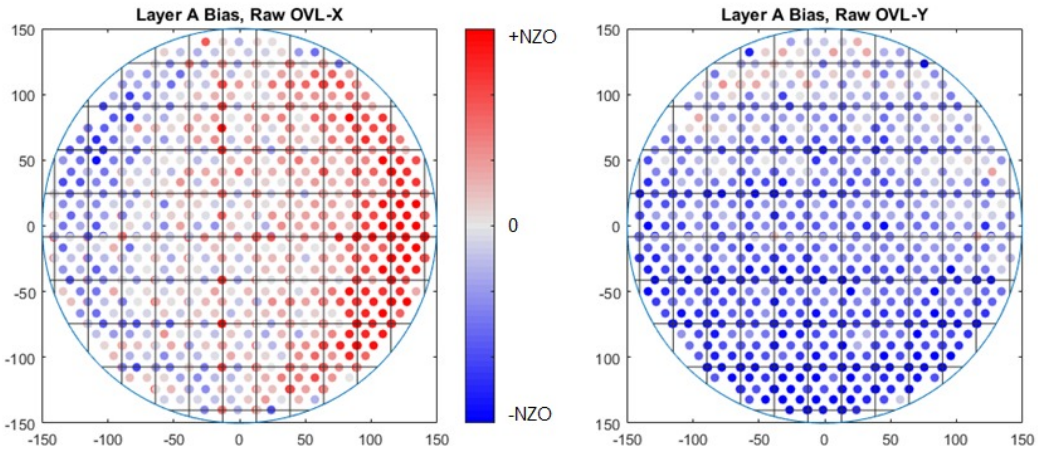

Figure 6: Full map DI-FI bias for Layer A, showing the raw (un-modeled) signature.

Analyzing further the Layer A full wafer DI-FI data, we perform a sources-of-variation analysis by modeling sequentially with higher order models. As shown in Figure 7, we can see that most of the variability can be characterized by a linear model W1F1. The next largest segment can be characterized by a third order model W3F3. Finally CPE6 and CPE 19 models are applied, with 6 and 19 terms per field, respectively. It can be seen that a significant portion of the variability beyond the high-order W3F3 POR model can be captured with CPE.

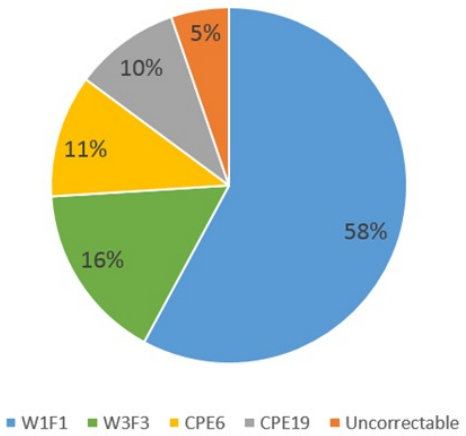

Figure 7: Layer A full map DI-FI bias sources of variation analysis including CPE.

4. CONCLUSIONS

DI-FI bias has been incorporated into process control for many nodes. What is new is the relative size of the NZO as compared to the overlay spec, and the need to find more comprehensive solutions to characterize and minimize the variability of the NZO. In this study we investigated a scheme for automated updates of NZO in the DI control loop based on low frequency FI updates. We demonstrated that a large portion of the DI-FI bias is common from lot-to-lot over a period of weeks but the lot-to-lot variation can also be significant on some layers, thus requiring careful consideration. Further work is underway to minimize NZO, to minimize NZO variability, to track NZO excursions, and to provide optimal NZO process control.

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