Stack and topography verification as an enabler for computational metrology target design

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ABSTRACT

Computational metrology target design requires both an accurate metrology simulation engine and an accurate geometric model. This paper deals with the later. Optical critical dimension metrology and cross-section SEM are demonstrated as two useful methods of geometric model verification with differing capabilities. Specifically, a methodology is proposed which allows the metrology engineer to quantify the level of accuracy required by the model as a function of the tolerable uncertainty in the prediction of metrology performance metrics. The methodology identifies a subset of model parameters which need to be verified enabling the metrology engineer to invest the minimum effort in stack and topography verification which will lead to performing target designs on the first design round.

Keywords: overlay metrology, computational metrology target design, stack and topography verification

1. INTRODUCTION

The pushout of EUV has set the stage for double and quadruple patterning to dominate the 10 and 7 nm nodes. This has major ramifications for metrology target design. The number of layers per stack, even for what was previously considered a single patterning step such as the poly layer has compounded. Since overlay metrology needs to probe both current and previous patterned layers, the effects are two-fold. Firstly, the previous layer is now buried under complex strata of functional and sacrificial layers, each of which may suffer from surprisingly large process variations at least in the process development stages when targets are designed. Secondly, in order to probe the underlayer, in many cases, metrology wavelengths have been driven into the near infra-red to penetrate multiple carbon and sometimes silicon based hard masks, BARCs and photo-resists.

Pupil and real imaging based metrology methods rely on collection of at least two diffraction orders [1], so Bragg’s law dictates a widening gap between measureable target pitches and device design rule pitches. These large pitch target structures are not high on the agenda of process integration teams who are primarily focused on optimizing advanced processes for single digit nanometer features. For several generations now target designs have become more complex in an attempt to maintain process compatibility as the gap widens between minimum device pitch and target pitch. Parallel and orthogonal feature segmentation are familiar strategies to all metrology engineers but to these have been added under and intermediate layer dummification and more recently CMP assist features. The space of a target Design of Experiment (termed t-DOE) has become enormous when process variations and their impact on precision and accuracy are to be taken into account in simulations comparing various geometric design contenders.

CMP dishing and induced topography may also affect metrology performance. If one wants to predict accuracy, precision and in particular process robustness as a function of geometry and wavelength, one needs to know the magnitude, or at least, the presence or absence of these process effects. So in this paper we shall focus on a comparison of different methods for stack and topography verification in advanced processes but in the practical light of a real process development environment. Methods characterized will include cross-section SEM (CS-SEM), and optical critical dimension (OCD) on dedicated targets. The improvement in matching between simulation and measurement resulting from stack and topography verification will be quantified.
2. THE METROLOGY TARGET DESIGN CYCLE

In the majority of advanced IC manufacturing processes today, the final version of the metrology and test structures are the result of a number of design iterations usually performed on test vehicles in the process development phase of the new product. Even the first design iteration is likely to share significant process characteristics with its predecessor at a previous node. This dictates that advanced target design methodologies are fundamentally cyclic in nature. Since computation based design [2] requires an accurate model of the stack and topography, these iterations are a crucial opportunity to tune the model in order to enable high fidelity predictions of metrology performance and ultimately enable the selection of a top performing target/setup contender. Figure 1 is a depiction of a design cycle used in advanced fabrication facilities today.

Figure 1: The metrology target design cycle includes 4 phases, (i) modeling and process variation estimation, including the model verification step, (ii) optimize which includes uncertainty analysis to determine impact of process variations, ranking and target diversification, (iii) measure which includes both optical metrology measurements and possibly accuracy verification measurements, and (iv) simulation to measurement (S2M) matching in which the model is compared with actual measurement in terms of optical signals and metrology metrics.

In the first phase a model is constructed based on available stack and topography information. This must necessarily include the specific design rules on a per layer basis to ensure that the target design of experiment (tDOE) includes multiple geometric contenders which are compatible with lithographic and process driven considerations. The simulation must additionally span the space of possible process variations, termed the Pvar domain. These two requirements can cause the number of permutations to rapidly grow and requires optimization. This point will be addressed in a later section. The relationship between the target design of experiment and process variation domain is illustrated in figure 2.
Activities in the design cycle subsequent to GDS file submission are not covered in this publication, but subsequent to tape-out the design will eventually reach silicon and the chuck of the metrology tool. Simulations are then compared with measurement (termed S2M matching) and the model may be further optimized to enable matching. The design cycle is complete when the improved model is used for a subsequent design cycle.

3. METHOD

In order to characterize the impact of stack and topography verification on the quality of the computational model, measurements and simulations were performed on 3 different stacks of increasing complexity. See Figure 2. Since the objective of the investigation was to determine the impact of verification on computational models in the aid of metrology target design, Scatterometry overlay (SCOL) measurements were performed on the Archer 500LCM metrology tool on overlay metrology targets of known design on 3 representative wafers for each stack. The 500LCM is a differential 1st order diffraction based pupil imaging system, described in reference [1]. The measurements allowed both pupil images from the targets to be collected in addition to metrology performance metrics. The 3 metrology performance metrics which were calculated were diffraction efficiency, i.e. the intensity ratio between zero and first orders in the pupil image, sensitivity, a metric indicating the relative change in the differential signal between diffraction orders and cells for a change in overlay, and ANRA (Adaptive Noise Reduction Algorithm) precision or repeatability of the measurement. The 2nd and 3rd metrics are not relevant for the first (single grating) target type since overlay metrology requires a grating over grating structure. Subsequently, a nominal stack model was built for all cases, using AcuShape software for geometric models, the nominal model was then perturbed with suspected process variations, uniquely for each stack. A preliminary attempt at matching the resultant simulated pupil images with the measurement pupil image was then performed. A software tool was developed, termed Simulation to Measurement (S2M) matching, which runs on all measurements and compares each measurement to a set of possible simulations. Among the outputs of the S2M software are curve fitting merits, such as $\chi^2$ as well as merits related to metrology performance.
Figure 3 Geometric stack description of three test cases. (a)-(b) side view and front view of the single grating model. (c)-(d) side view and front view of resist over etched silicon in a grating over grating configuration. (e)-(f) side view and front view of a multi-layered structure in a grating over grating configuration.

In a next step stack and topography verification was performed on the wafers. Two characterization methods were used: film optical properties (n&k) and optical critical dimension (OCD) metrology [3] and cross-section scanning electron microscopy (CS-SEM) [4]. OCD metrology is a non-destructive scatterometric method that allows monitoring and characterization of various complex three dimensional shapes starting from front-end layers to the last interconnect layers. OCD metrology can be performed using a diverse array of optical technologies such as: spectroscopic ellipsometry (SE), polarized enhanced ultra-violet reflectometer (eUVR), multi-azimuth scatterometry and multi-channel scatterometry. Due to its destructive nature, CS-SEM is not used for HVM, but for reliability and R&D purposes. CS-SEM is a powerful technique, which enables revelation of the structure with a resolution of less than 1 nm. Figure 4 illustrates the output of OCD metrology showing the measured and modelled spectra (b) and the geometric model (a). A CS-SEM image and the geometric models before and after verification are shown in Figure 5(a) and Figure 5(b), respectively. Figure 6 shows the geometrical model of the multi-layer stack, before and after cross-section SEM verification (not shown). Significant topographic differences can be observed in the model, in particular the presence of induced topography which significantly modifies metrology performances between setups. The next step was to perform a second comparison between the measured and simulated pupil images. Although it is in principle possible to obtain correct target contender ranking without achieving an excellent match between simulation and measurement, performing S2M is an important step for target design verification subsequent to process uncertainty analysis.
Figure 4(a) single grating model for model based OCD measurement with several degrees of freedom. (b) measured and simulated spectroscopic ellipsometry output for CD and film verification.

Figure 5 (a) CS SEM image of the stack topography, (b) nominal geometric model. (c) Detailed geometric model based on CS-SEM.

Figure 6: Multi-layer grating over grating model before and after cross-section SEM verification. Note changes in induced topography, CD biases and number of layers.
4. RESULTS

Figure 6 (a)-(f) shows the post verification geometrical models for a single diffraction grating, simple resist over etched silicon grating-over-grating scatterometry overlay target and a multilayer grating-over-grating scatterometry overlay target. In all three cases, pupil image scatterometry measurements were collected and analyzed and then compared to the simulations spanning a range of process variations. Both measurements and simulations were performed at multiple tool recipe setups spanning changes in illumination wavelength, apodization and polarization. In figure 7 & 8 the match between simulation and measurement is quantified by taking pupil cross-sections and calculating $\chi^2$, defined by

$$
\chi^2 = \sum \frac{(\text{measured} - \text{simulated})^2}{\text{simulated}}
$$

Based on experimental results, good matching is indicated by $\chi^2$ in the range of 10 to 20, while excellent matching is defined as $\chi^2$ less than 10. The level of confidence in the simulator and the geometric model will be high if good to excellent matching is achieved over multiple tool recipe setups simultaneously.

It is evident in the case of the single grating structure that a reasonable match was already obtained using the nominal grating model. Nonetheless, subsequent to model refinement including optical characteristics n&k, $\chi^2$ was below 10 in all recipe setups.

![Figure 7](image_url)

Figure 7 Measured and simulated pupil image cross sections of a single grating structure. (a)-(c) & (g)-(i) cross sections before and (d)-(f) & (j)-(l) are after OCD verification at different measurement and simulation setups.
As shown in figure 7, for the grating over grating case, the pre-verification simulated pupil image cross sections were significantly different from the measured signals indicating significant inaccuracies in the nominal model. However, subsequent to cross-section verification, a marked improvement in the matching is observed, with 5 out of 6 of the recipe setups showing $\chi^2$ matching values below 20.

Before | After | Before | After

![Graphs showing before and after comparison](image)

Figure 8 Measured and simulated pupil image cross sections of a simple grating-over-grating structure (a)-(c) & (g)-(i) cross sections before and (d)-(f) & (j)-(l) are after CS SEM verification at different measurement and simulation setups.

![Comparison tables](image)

Figure 9 Example measured and simulated comparisons of diffraction efficiency (DE) and chi square ($\chi^2$) for the first two test cases, (a) is single grating, (b) is grating over grating.
Figure 10: S2M matching drilldown for multi-layered grating. Measured vs simulated performance metrics. Results are shown for Diffraction Efficiency, Sensitivity and ANRA precision. Color coding is as follows: Green means both Meas. MAX <= Sim. MAX & Meas. MIN >= Sim. MIN. Yellow means either Meas. MAX > Sim. MAX or Meas. MIN < Sim. MIN. Red means either Meas. MAX & Meas. MIN < Sim. MIN, or Meas. MAX & Meas. MIN > Sim. MAX. In the case of ANRA precision, the simulated results represent a lower bound of the measured precision. In all cases, simulated is lower than measured precision.

Figures 9 & 10 show additional indicators of S2M matching. Although pupil image matching is a strong indicator of model fidelity, metrology target design contenders are ranked based on predicted metrology metrics, including diffraction efficiency, sensitivity and precision, specified in section 3 above. Comparing these metrics between simulation and measurement requires consideration of process variations which, as will be discussed in more detail below, can have a significant impact on metrology metrics. If our model and the process variation bounds have been correctly defined, then it is anticipated that the range of measured values for the metrics will be bound by the maximum and minimum values of the simulated metrics over the range of process variation. The exact methodology of S2M matching quantification is specified in the figure caption of figure 9. The results in figure 10, for a realistic multi-layer stack are at a level which provides high confidence that the model will enable scatterometry overlay metrology design with predictable performance.
5. UNCERTAINTY ANALYSIS

A key question which needs to be addressed when performing stack and topography verification, is “when is the model accurate enough?” Uncertainty analysis is a methodology which enables quantification of the impact of stack and topography uncertainty on the predicted metrology metrics. In uncertainty analysis, for a given geometric target design, the impact of a user specified process variation is determined for each metrology metric by calculating the value of the metric from pupil images at the edge of each process variation range and comparing with the value of the metric for the nominal, unperturbed geometry. This analysis provides the designer with quantitative feedback to be used in 4 ways:

1. restrict stack and topography verification to process parameters with the greatest influence on target metrics,
2. build a computationally compact simulation by removing Pvar parameters which do not impact metrology performance metrics,
3. provide the user with quantitative data on the impact of process variations on metrology performance to support his dialogue with process integration and
4. provide an indicator for S2M matching expectations.

An example of the impact of each process variation on overlay metrology accuracy is shown in figure 8 below.

Figure 11: Uncertainty analysis for the multi-layer example, showing impact of each process variation on metrology precision. Such analysis can be extended to all metrology metrics. The blue circle in this chart indicates the precision (in Ångstroms) for the nominal, unperturbed geometry. The green area indicates how a user defined process perturbation modified the simulated precision for each stack and topography parameter. Parameters for which there are large swings in the green boundary away from the blue circle indicate stack or topography parameters in the model which require greater attention in verification since they are more likely to impact performance.
6. CONCLUSIONS

Metrology simulations have played a role in target and sensor design for over a decade [5], [6]. At the outset of this work, extensive experience in the verification of metrology simulation platforms had already demonstrated that it is not enough to validate the simulation platform – the model also needs to achieve a level of accuracy, determined by the purpose of the simulation. Beyond this, the conclusions of the work presented in this publication are as follows:

1. Independent verification methods are required in order to achieve a level of model accuracy that enables simulation based target design.
2. Optical film and critical dimension metrology can be used to provide verification of basic stack and topography parameters such as thickness, n&k, CD and sidewall angle.
3. Cross-section SEM metrology can be used to provide verification of basic stack description, presence or absence of features such as dishing & induced topography.
4. In addition to model accuracy, metrology simulation based target design must efficiently span the domain of metrology tool recipe, target geometry and process variations in a computationally compact fashion.
5. Uncertainty analysis can identify which of a myriad of stack and topography parameters really matter – where should the metrology engineer invest his very limited time and resources in verification.

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