Reflective electron-beam lithography performance for the 10 nm logic node

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ABSTRACT

Maskless electron beam lithography has the potential to extend semiconductor manufacturing to the sub-10 nm technology node. KLA-Tencor is currently developing Reflective Electron Beam Lithography (REBL) for high-volume 10 nm logic (16 nm HP). This paper reviews progress in the development of the REBL system towards its goal of 100 wph throughput for High Volume Lithography (HVL) at the 2X and 1X nm nodes. In this paper we introduce the Digital Pattern Generator (DPG) with integrated CMOS and MEMs lenslets that was manufactured at TSMC and IMEC. For REBL, the DPG is integrated to KLA-Tencor pattern generating software that can be programmed to produce complex, gray-scaled lithography patterns. Additionally, we show printing results for a range of interesting lithography patterns using Time Domain Imaging (TDI).

Previously, KLA-Tencor reported on the development of a Reflective Electron Beam Lithography (REBL) tool for maskless lithography at and below the 22 nm technology node1. Since that time, the REBL team and its partners (TSMC, IMEC) have made good progress towards developing the REBL system and Digital Pattern Generator (DPG) for direct write lithography. Traditionally, e-beam direct write lithography has been too slow for most lithography applications. E-beam direct write lithography has been used for mask writing rather than wafer processing since the maximum blur requirements limit column beam current - which drives e-beam throughput. To print small features and a fine pitch with an e-beam tool requires a sacrifice in processing time unless one significantly increases the total number of beams on a single writing tool. Because of the continued uncertainty with regards to the optical lithography roadmap beyond the 22 nm technology node, the semiconductor equipment industry is in the process of designing and testing e-beam lithography tools with the potential for HVL.

1. INTRODUCTION

The Reflective Electron Beam Lithography (REBL) tool currently under development at KLA-Tencor for DARPA (MTO) is designed for custom ASIC processing. Corporate development efforts over the past three years have also focused on developing a tool for HVL. The system currently under development is targeting critical patterning steps at the sub 22 nm technology node at a capital cost equivalent to 0.5 MS/WPH. As noted in earlier work1, the patented, reflective electron optic or DPG enables the REBL system to produce a massively parallel lithographic exposure using well over a million electron beams. The DPG is a CMOS ASIC chip (from TSMC) with an array of small, independently controllable lens elements (lenslets), which act as an array of electron mirrors. In this way, the REBL system is capable of generating the pattern to be written using massively parallel exposure by ~1 million beams at extremely high data rates (~1Tbps). The lens elements on the DPG are fabricated at IMEC (Leuven, Belgium) under IMEC’s CMORE program. To drive throughput and reduce overall system risk, the REBL team has plans to implement multiple DPGs (multiple-columns) and replace a previously planned rotary stage concept with a dual action, linear stage technology. This new multi-column and linear stage architecture has the potential to produce wafer throughputs exceeding current 193 nm immersion lithography systems. The new linear stage design also has the added benefit of reduced system vibration and cancellation of stage acceleration forces. This work is supported by DARPA under contract HR0011-07-9-0007.
Electron Beam Lithography (EBL), since its beginning, has fallen short in lithography for HVL because of insufficient throughput - except for mask making\textsuperscript{2}. High resolution lithography and customization for specialized products\textsuperscript{3} are other areas where Electron Beam Direct Write (EBDW) has proven useful. For these applications both resolution and maskless imaging have been more important than throughput. Quick-turn-around\textsuperscript{4,5} and small lot manufacturing\textsuperscript{6} have also proved to be quite successful applications of EBDW. SCALPEL\textsuperscript{7} and PREVAIL\textsuperscript{5,9} were two competing electron projection lithography programs that demonstrated very good progress but did not utilize one of EBL’s most important assets, namely, maskless imaging. Currently, there are three major maskless EBDW programs under development: MAPPER\textsuperscript{10}, IMS\textsuperscript{11}, and REBL\textsuperscript{12,13}. The program at KLA-Tencor is jointly funded by KLA-Tencor and DARPA, under the Maskless Nanowriter Program. For DARPA applications, the REBL tool is designed to direct write 5-7 wafer layers per hour for the 45 nm node. This report summarizes work for extending the technology for HVL 10 nm technology node (logic, 16 nm HP). Figure 1 shows a CAD layout of the REBL electron beam optics integrated to a linear stage concept that will be part of a HVL system.

![Digital Pattern Generator: DPG, Illumination Optics, Demag Optics, Electron Gun, Projection Optics, Multiple Wafers, Linear Stages](image)

**Figure 1.** REBL linear stage concept; multiple wafer stage, DPG, and beam optics

### 2. REBL ARCHITECTURE FOR HVL

Over the past year, KLA-Tencor has investigated several different stage and e-beam column configurations (for example, see Figure 2) that have the potential for HVL for the 10 nm technology node (logic, 16 nm HP). Since a single REBL column will not provide the throughput needed for HVL the REBL team continues design work for a multi-column prototype system (Figure 3 below). As the number of columns increases many other system requirements are significantly reduced. A larger number of columns allows for a lower writing speed, reducing the requirements on
current through a single column, stage speed, etc. The key then, is to make the electron optics small, simple, reliable, and inexpensive enough to replicate many times per cluster. Increasing the number of columns allows us to concentrate complexity into things which scale well, like the DPG, rendering algorithms and stage positioning and beam positioning algorithms. The DPG leverages CMOS technology and infrastructure, which should scale with device node. The rendering algorithms leverage HPC infrastructure, which also improves with increasing shrinks of chip design. Our stage control and beam positioning algorithms leverage HPC, DSP, and FPGA. By contrast, things which are traditionally complex in litho systems are comparatively simple, for example the optics, stage and source are all readily available.

The optimum REBL architecture for HVL still has at its foundation the concept of reflective electron optics. The reflective optics were chosen because of their compact form of while still generating $10^6$ beamlets in a single column, even though this limits the usable beam current to single digit microamperes due to beam blur from Coulomb interaction between electrons. It was determined that this was a reasonable trade-off when other system issues are taken into consideration. Some of these other system issues are calibrations, sensitivity to electromagnetic interference, heating effects, data path architecture, and electron optics field of view. For HVL lithography, the REBL system currently in design will use multiple e-beam columns and a dual action linear stage technology (Figure 2). The system for HVL at the 10 nm logic node is envisioned to have 36 e-beam columns and several dual action linear stages as shown in Figure 3.

The key advantages of moving to a multiple column and linear stage architecture for HVL direct write are:

- Systems modeling shows that the wafer throughput for HVL can be met
- The multi-column linear stage design operates at a linear velocity of ~1 m/s vs. 10 m/s for a system with fewer columns and rotary stage. At lower velocities the linear stage design offers similar/improved throughput as compared to rotary operation
- The linear stage simplifies stage design and stage metrology
- Dual opposing stages minimize vibrations due to stage accelerations
- The data path and rendering algorithms for writing are simplified and data can be re-used
- Multiple columns enable sufficient beam current at the required beam blur specifications
- The design supports a COO that is comparable to or better than EUV litho near and below the 16 nm node

The writing strategy for the HVL system is still based on proven TDI exposure architectures, allowing for writing on a continuously moving stage for minimal stage overhead. The small writing area minimizes blur and placement errors from across-swath distortions like thermal expansion, differential magnetic fields, power supply drift, and stage yaw. The design also allows for real time, as needed, correction of global wafer expansion. The ~100 keV exposure energy enables high aspect ratio patterning of resist for simple processing and minimizes charging-induced placement errors.

Figure 2. REBL HVL Concept; showing two columns and one dual action stage
The following table (Table 1) shows a comparison of the REBL linear vs. rotary design to meet the requirements for HVL at the 10 nm logic technology node. These results are based on system simulations for the different use cases, stage design, resist sensitivity, and expected stage accelerations and velocities. Our calculations show that the new linear stage design is generally equal in throughput to a rotary platform.

<table>
<thead>
<tr>
<th></th>
<th>Linear, $30 \mu C/cm^2$ resist</th>
<th>Rotary, $30 \mu C/cm^2$ resist</th>
<th>Linear, $60 \mu C/cm^2$ resist</th>
<th>Rotary, $60 \mu C/cm^2$ resist</th>
</tr>
</thead>
<tbody>
<tr>
<td>All Critical Layers</td>
<td>43 wph</td>
<td>47 wph</td>
<td>24 wph</td>
<td>22 wph</td>
</tr>
<tr>
<td>Line Cutting</td>
<td>90 wph</td>
<td>93 wph</td>
<td>53 wph</td>
<td>52 wph</td>
</tr>
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### 3. REBL DIGITAL PATTERN GENERATOR WITH CMOS AND LENSLETS

During the past year, KLA-Tencor has worked closely with TSMC and IMEC (Leuven, Belgium) to produce functional CMOS DPGs. The latest DPG chips (248 x 4096 mirror array at 1.6 $\mu$m pitch) from IMEC have been integrated to the 75 kV column and fine tuned to optimize imaging in both PMMA and CAR films. For the 16 nm HP logic node the team is in the process of building a 100 kV column that will operate with a beam current $\geq 1$ $\mu$A. The team is also working on a DPG3 version that will have a 248 x 4096 lenslet array with integrated data compression that can be addressed in rows. These DPG modifications will enable the DPG to write data in both directions which is needed for HVL applications. The current DPG2 chip is shown attached to the DPG board assembly in Figure 4 below. The custom ceramic board has 28 metal layers and provides over 1000 interconnects for the 1454 DPG bond pads. Once packaged, the DPG is integrated into the REBL system and fine tuned for optimized imaging performance. For future HVL manufacturing, the REBL system could be configured with over 100 DPGs and columns (Figure 3 above shows a configuration of 36 total columns and DPGs).
6. REBL E-BEAM COLUMN AND YAG IMAGES

After DPG integration onto the 75 keV column, the DPG and column electronics are fine tuned for both static and TDI exposures. Currently, REBL experimental columns are configured with novel diagnostic optics for characterizing DPG chips, verifying optical performance (resolution and contrast), beam alignment, and focus. The diagnostic tool or Mag Stack consists of an electron microscope stack below the wafer plane to magnify the aerial image to a YAG screen. During REBL tuning operations, the e-beam and resulting aerial image can be projected onto the YAG screen to view the aerial image at the wafer plane and produce high resolution images of the DPG mirror pixels. Figure 5 below shows a YAG image of the DPG mirror array where a magnified, 20 nm pixel (pitch) is clearly visible. Figure 6 shows a large portion of the entire DPG array on the YAG screen where both line and space and lithography target patterns are displayed.
**Figure 5.** REBL DPG pixels imaged on the mag stack YAG screen

**Figure 6.** REBL DPG line and space pattern (L) and test targets (R) using the mag stack YAG
7. TDI IMAGING RESULTS AND FUTURE WORK

The second generation REBL column has now been integrated with a precision controlled wafer stage at KLA-Tencor (Milpitas CA). The team is currently running both static and dynamic (moving wafer stage) TDI lithography exposures using both PMMA and Chemically Amplified Resist (CAR) films. With a 75 keV column (and 87X demagnification) the REBL team has produced several different contact arrays down to a 28 nm half pitch (Figure 7 below). The DPG can be programmed for Time Domain Imaging (TDI) to produce exposures on a moving stage. During TDI exposure, the DPG is continuously updated (pixels are turned off or on as needed for exposure control) in the 248 pixel direction as the wafer stage moves. CAR films with <18 \( \mu \text{C/cm}^2 \) sensitivity and sub-45 nm resolution capability are currently being explored for TDI exposure. Figure 8 shows TDI exposure results for 100 nm wide chevron patterns in PMMA resist. The ability of the REBL tool to produce a wide variety of lithography patterns without a lithography mask is clearly demonstrated in the images below.

![Image](http://example.com/image.jpg)

**Figure 7.** REBL DPG contact hole arrays showing contact holes at 37 nm and 28 nm half pitch in PMMA.
8. SUMMARY

- The REBL architecture has the potential to provide a HVL solution at 16 nm and beyond
- We have adopted a new linear stage that minimizes program risk, simplifies system design, and maintains HVL throughput capability
- KLA-Tencor throughput calculations support current design decisions
- KLA-Tencor optical simulations support HVL capability through at least the 16 nm HP node (logic)
- TDI printing on a moving wafer stage has produced a wide variety of grey-scaled lithography patterns.

9. ACKNOWLEDGEMENTS

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REFERENCES