REBL: design progress toward 16 nm half-pitch maskless projection electron beam lithography

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ABSTRACT

REBL (Reflective Electron Beam Lithography) is a novel concept for high speed maskless projection electron beam lithography. Originally targeting 45 nm HP (half pitch) under a DARPA funded contract, we are now working on optimizing the optics and architecture for the commercial silicon integrated circuit fabrication market at the equivalent of 16 nm HP. The shift to smaller features requires innovation in most major subsystems of the tool, including optics, stage, and metrology. We also require better simulation and understanding of the exposure process.

In order to meet blur requirements for 16 nm lithography, we are both shrinking the pixel size and reducing the beam current. Throughput will be maintained by increasing the number of columns as well as other design optimizations. In consequence, the maximum stage speed required to meet wafer throughput targets at 16 nm will be much less than originally planned for at 45 nm. As a result, we are changing the stage architecture from a rotary design to a linear design that can still meet the throughput requirements but with more conventional technology that entails less technical risk. The linear concept also allows for simplifications in the datapath, primarily from being able to reuse pattern data across dies and columns. Finally, we are now able to demonstrate working dynamic pattern generator (DPG) chips, CMOS chips with microfabricated lenslets on top to prevent crosstalk between pixels.

Keywords: ebeam, electron beam lithography, direct write, maskless lithography, resist, parallel lithography

1) INTRODUCTION

REBL (Reflective Electron Beam Lithography) is a novel approach to high-throughput maskless electron beam lithography that uses a reflective dynamic pattern generator (DPG) chip to modulate the aerial image of a large area electron beam that is projected onto the wafer. REBL has several key technological concepts that are shown in Figure 1. The DPG chip is floating at the cathode potential which reduces power dissipation from the electron beam to the microwatt level. It also allows the DPG to modulate the electron beam aerial image with only 2 volts change of electrode potential. This is easily supplied by CMOS circuitry which is placed underneath each pixel, also allowing a dense “brush” of pixels. The dense brush minimizes the field size of the optics, and reduces thermal, mechanical, and illumination variations across the pixel array, while also reducing the total illumination current needed for a given current at the wafer. The data scrolls across the DPG in synchronicity with the stage motion, thus each “brush” draws a swath of exposed images across the wafer. This time domain integration (TDI) writing mode has a number of significant architectural advantages. Because each pixel on the wafer is exposed by multiple pixels on the DPG, pixel to pixel variations are averaged out, and even a dead pixel can be tolerated, providing redundancy. In addition, each pixel can be turned on and off during part of the time it scrolls across the DPG, thus allowing dose modulation on a per-pixel basis.
with 31 gray levels. The projection optics is responsible for demagnifying the DPG image by about 100X onto the moving stage. A wafer metrology system (WMS) optically measures the wafer position for accurate overlay without exposing the resist.

Figure 1. Schematic diagram of REBL system showing key subsystem blocks including the DPG, optics, stage, and WMS alignment sensor.

The REBL project originally targeted the 45 nm (half-pitch) node and some key architecture choices were made based on this assumption. The current plan is to introduce the REBL tool at the 16 nm (half-pitch) node, which will require fundamental architecture changes.

Foremost among the changes is a switch from a rotary to linear stage architecture. Original projections for stage speed at the 45 nm node required a rotary stage because the turn-around time from a linear stage would adversely impact throughput. At the 16 nm node, linear writing speeds are significantly reduced and a linear stage is projected to have equivalent throughput to the rotary stage. However, the linear stage has lower costs both for the stage and other subsystems, and also entails less risk because it is a much better understood technology. A corollary to the slower writing speed is a requirement for more columns in order to reach a 100 wafer/hour throughput target. The linear stage system will hold multiple wafers and may incorporate multiple stages for increased throughput. Each wafer will be
written by a single column on the initial pre-alpha tool, but the high-volume manufacturing (HVM) tool will incorporate multiple columns per wafer.\footnote{DPG DEVELOPMENT}

Metrology requirements are also much tighter for the 16 nm node. A total metrology budget of 1 nm (3 sigma) has been established which places sub-nm positional requirements not only on the stage, but also on the wafer position measurement for overlay.

For the optics, we are making incremental improvements in column performance in order to meet 16 nm requirements. The changes include increasing the beam energy to 100 keV, as well as improved lens designs to reduce aberrations and increased demagnification ratio for smaller pixels at the wafer.

2) DPG DEVELOPMENT

The DPG consists of an array of 248 by 4096 pixels, each pixel separately controlled by a CMOS circuit underneath the pixel. On top of the pixels is an array of microlenses that serve to eliminate electrical crosstalk between pixels. The microlenses also provide optical matching between the DPG and the projection optics. By switching the voltage of the electrode at the bottom of the microlens, electrons from the illumination beam can be either reflected back into the projection optics (“on” pixel) or absorbed by the bottom electrode (“off” pixel). We have built working arrays of lenslets without CMOS that we call static DPG chips shown in Figure 2, and demonstrated the ability to print features smaller than 45 nm in PMMA resist.\footnote{Figure 2. Cross section of a static lenslet array fabricated on a silicon wafer.}

We have previously designed and built working CMOS DPG chips without lenslets. We have also now integrated the lenslets on top of the CMOS and shown functional chips, although we are still debugging some process issues that are impacting yield and performance. In addition to the chip fabrication itself, bonding and wiring the chip into a vacuum-compatible package also poses significant challenges. Figure 3 shows a focused ion beam cross-section of a completed DPG with the lenslets visible on top of the CMOS metal layers. Figure 4 shows a checkerboard electron image from a CMOS DPG installed onto a system and projected onto a YAG fluorescent screen. In real time we have demonstrated

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the ability scroll arbitrary patterns across the DPG chip. We are now working on coordination with the stage motion so that we can demonstrate printing of arbitrary patterns in resist.

Figure 3. Focused ion beam cross section of a CMOS DPG showing lenslets fabricated on top of CMOS circuitry.

Figure 4. Electron beam aerial image modulated by the CMOS DPG and projected onto a YAG screen. The imaged area is 248 by 256 pixels.
3) STAGE REQUIREMENTS AND DESIGN

When originally developed for the 45 nm node, REBL’s stage speeds were predicted to be as high as 10 m/s. A traditional linear stage shuttling back and forth would suffer unacceptable acceleration or turn-around times at those velocities, so a continuous motion rotary stage concept was developed. However, for the 16 nm node, where pixel sizes and beam currents are smaller, we will use multiple columns to achieve throughput, so the maximum speed required by each column is correspondingly reduced. As a result the maximum stage speed is now not expected to exceed 1 m/s. At these speeds, the requirements can be relatively easily met by a linear stage.

We are evaluating several concepts for the stage. These include either a mag-lev or air-bearing design; opposing counter-moving stages to minimize inertial excitation to the system; and stages that carry multiple wafers for higher throughput. Prototype tools will utilize one column per wafer. We are starting development of a column small enough that up to 6 columns can be placed over each wafer, allowing an additional improvement in throughput needed for high volume manufacturing.

The metrology for the stage must be capable of determining the stage position to within a nanometer in real time. Current plans are to use a conventional multi-axis interferometer system. The wafer rotation must be settable to a high degree of precision so that each swath runs exactly parallel to any existing patterns on the wafer. This requirement allows the datapath to re-use swath data from die to die. Errors in stage position are measured and fed to the column electronics to correct beam position in real time. A wafer metrology system (WMS) measures the wafer position with nanometer precision using non-actinic light so as not to expose the resist. Figure 5 shows a block diagram of the major stage components for a prototype system with two stages, two wafers, and two columns.

4) DATAPATH DEVELOPMENT

The data preparation software together with the datapath are responsible for formatting the design data, implementing proximity corrections and other shape corrections, formatting the data as needed by the DPG, and delivering the data to the DPG at the time needed for writing on the wafer. For the rotary stage concept, every swath was unique, requiring much of the data processing to be done in real time. With the linear stage, we can determine swath position ahead of time, allowing steps such as rendering the data into gray levels to be done as a pre-process step. In addition, because the swath covers multiple dies across the die row, and repeats from die row to die row, there is opportunity for data re-use both within a swath and from swath to swath. Data re-use dramatically reduces the overall computational requirements for the datapath.

Data preparation begins with layer extraction from a GDSII or OASIS design file. Proximity correction is applied using simplex-based methods. Previous layer data will be taken into account as needed to allow for variations in the backscatter coefficient. The data is then formatted into an intermediate compressed format that can be stored for future use.

The next step is to render the data, or convert it into pixels with gray level assignments. This step is also performed offline, starting with the proximity-corrected data. The converted pattern is then compressed prior to being sent to the lithography system for writing. Various lossless compression techniques have been previously demonstrated. The final step is to distribute the gray level pixel data to each DPG during the writing process as required by the print cycle.
5) EMULATION OF REBL PRINT STRATEGY

In order to confirm that the REBL writing strategy can achieve sub-pixel pattern placement, edge placement/CD control, and line edge roughness control, we devised a test pattern consisting of verniers containing lines with sub-pixel spacings: a reference array of lines with a 150 nm pitch which is placed right above another array with a 151 nm pitch and the same linewidth. The nominal linewidth varied from 40 nm to 50 nm. Figure 6 shows an SEM micrograph of the test pattern exposed to perform the experiment. The placement accuracy can be measured by comparing the position of the test line to the position of the corresponding reference line, the ideal relative placement is given by the line number times the pitch difference.

The pattern has been fractured into single 20 nm pixel intensities calculated using a simplex based method\textsuperscript{5, 6}; the normalized dosages have been discretized into 32 gray levels including zero. The resulting set of pixels has been converted into an array of single point exposures defined on a 20 nm rectangular grid. The exposure has been performed by a vector scan 100 keV electron beam system using a beam diameter that was varied from 30 to 45 nm. Thus the grid, gray levels, feature size, and beam blur are all consistent with a REBL tool set up for 45 nm lithography. The exposed sample is bare silicon wafer with a 50 nm PMMA layer, developed in a 1:1 solution of water and IPA yielding a high contrast resist image.
Figure 6. Vernier pattern used to validate the ability of REBL to place features with sub-pixel accuracy. The upper lines have a 150 nm pitch, the lower lines have a 151 nm pitch. The print was done with a gaussian beam electron beam lithography tool configured to match the expected characteristics (blur, pixel size and dose levels) of REBL configured for 45 nm lithography.

The feature placement accuracy has been measured as a difference between the center of gravity of the test line and the center of gravity of the reference line based on SEM image analysis; this variable is plotted against the center of gravity of the reference line in Figure 7. Ideally the theoretical slope of the line in the figure should be the incremental shift per line (1nm) divided by the reference pitch or 1/150 = 0.006667; the slope resulting from the linear fit to the data is 0.0067 equal exactly to 1 nm increment. The error bars are the CD difference between the sample line and the reference line. Analysis of the data shows a 3 sigma pattern placement error of 2.0 nm, or 1/10 of a pixel. We plan to continue experiments to also measure CD control and line edge roughness.

6) OPTICAL DESIGN AND PERFORMANCE

In 2009, REBL optics changed from a magnetic prism to a wien filter based approach for separating the projection beam from the illumination for its 2nd generation optics. Since then we have continued to advance this optical concept with a 3rd generation column currently integrated on a rotary mag-lev stage. The third generation optical design is functionally similar but the beam energy has been increased from 50 keV to 75 keV. The increased beam energy reduces chromatic aberration and also reduces blur from coulomb interactions in the beam. Figure 8 shows a low current image from column 3 projected onto a YAG screen, with individual pixels on a 20 nm pitch clearly resolved.

We have used 2 methods to measure the actual blur in column 2 and column 3. On a test stand, we can incorporate a "mag stack", which is a set of 4 lenses below the image plane that can re-magnify the virtual wafer image onto a YAG fluorescent screen. The magstack itself adds additional blur and this must be taken into account when comparing experiment to simulation. Figure 9 shows the simulated blur with and without the mag stack, and the measured blur.
which includes the mag stack contribution, on column 3. There is excellent agreement between simulated and measured blur when the mag stack is taken into account.

![Offset vs Reference Position](image)

**Figure 7.** Results of the pattern placement emulation test demonstrating the ability to place features with sub-pixel accuracy. The measured 3 sigma error in placement accuracy is 2.0 nm, corresponding to a tenth of the 20 nm pixel.

![Mag stack image from column 3 with static DPG at low current](image)

**Figure 8.** Mag stack image from column 3 with static DPG at low current. Under these conditions individual pixels on a 20 nm pitch are clearly resolved.

The other way we have measured blur is to look at linewidth in resist as a function of dose and compared to simulation. The simulation is done for a range of beam blurs and assumes a Gaussian beam profile with a finite contrast level that includes both the contrast from our DPG as well as backscatter effects from electron interaction with the wafer. The
simulation also assumes a perfect resist with infinite contrast. Therefore, the blur measurement will incorporate resist resolution effects as well as aerial image blur. The simulations match experiment for a blur of 25 nm, which includes contributions from the optical blur, any noise and vibration, scattering in the resist, and the intrinsic resist resolution. Improved shielding and noise reduction on future systems will bring this number down to our entitlement.

![Graph showing blur vs. wafer plane current for different generations of columns.]

Figure 9. Comparison of experimental and simulated blur for column 3. If the additional blur from the mag stack is included in the simulation, the simulation and experimental results are in good agreement.

To reach 16 nm half-pitch, we are designing a 4th generation optical system. There will be 3 main improvements relative to column 3. First, the beam energy will be further increased to 100 keV. Second, the projection lens has been redesigned to have lower aberrations. Finally, we have dramatically reduced the size and length of the illumination optics. Previously, the illumination optics was so long that a bender section was required to prevent interference between the gun and the wafer. By shrinking the size of the gun and eliminating the separate condenser lens, we can now fit the illumination optics into the space between the wiener filter and the first magnetic demagnification lens. The schematic of the 3rd and 4th generation optics are compared in Figure 10.

In order to simulate the blur, we use MEBS software\textsuperscript{9}, primary the OPTICS module for geometric aberrations, and the IMAGE module for coulomb interaction blur. Results from IMAGE are shown in Figure 11 comparing the blur as a function of current for the latest 3 generations of columns. In order to print 16 nm half-pitch, we have a target blur of 11 nm (measured by the 20% to 80% rise across a sharp edge).

7) SUMMARY

REBL technology has been demonstrated for 45 nm level lithography. We have printed sub-45 nm features with a static DPG, demonstrating that the reflection concept with microlenslets works as expected. The CMOS DPG, which will be capable of printing arbitrary features, has been shown to be functional, and we expect to demonstrate printing of arbitrary patterns in resist in the near future.
We are now working on extending REBL technology to the 16 nm half-pitch node, where we plan for commercial introduction of a tool. A major change in tool architecture is the shift from a rotary stage concept to a linear stage. Because we will use multiple columns to achieve throughput requirements, the stage speed is reduced accordingly, obviating the need for the rotary stage. The linear stage will use more conventional technology, simplify the datapath,
and still be capable of meeting all requirements for the 16 nm node tool. We are changing the datapath design to take advantage of the simplification offered by the linear stage. Finally, a next generation column has been designed that will be capable of achieving the blur required for 16 nm printing. All these changes are now in the design stage for a pre-alpha tool.

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