Methodology for Overlay Mark Selection

Chin-Chou Kevin Huang*[a], Chao-Tien Healthy Huang[a], Anna Golotsvan[a], David Tien[a]
Chui-Fu Chiu[b], Chun-Yen Huang[b], Wen-Bin Wu[b], Chiang-Lin Shih[b]

[a]KLA-Tencor Corporation, 1 Technology Drive, Milpitas, CA, USA 95035;
[b]Nanya Technology Corporation, No. 98, Nanlin Rd., Taishan Shiang, Taipei County 24309, Taiwan

ABSTRACT

It is known that different overlay mark designs will have different responses to process setup conditions. An overlay mark optimized for the 45nm technology node might not be suitable for wafers using 30nm or 20nm process technologies due to changes in lithography and process conditions. As overlay control specifications become tighter and tighter, the process engineer requires metrics beyond precision, tool-induced shift (TIS) and TIS variability to determine the optimal target design. In this paper, the authors demonstrate a novel, comprehensive methodology which employs source of variance (SOV) to help engineers select the best overlay marks to meet overlay control requirements.

Keywords: Overlay, SOV, target design

1. INTRODUCTION

Overlay mark design and selection are the first two steps of overlay control. Some target designs are sensitive to lithography processes, typically showing differences in the field overlay error component. Certain target designs may be more sensitive to etch or CMP loading and may exhibit systematic wafer-level linear or high order overlay error components. Some targets can be easily damaged by processes and will result in higher statistical overlay error noise than other designs.

The same overlay mark used in the 45nm process node might not be suitable for the 30nm or 20nm process nodes due to changes in the processing of the wafer. Traditional overlay target selection mainly focuses on total measurement uncertainty (TMU) performance, which considers only precision, TIS variability, and tool-to-tool matching as described by Eq. (1):

$$\text{TMU} = \sqrt{(TIS3sigma)^2 + \text{Pr}ecision^2 + matching^2} \quad (1)$$

In addition to TMU, metrology engineers may also consider residual overlay error after removal of linear contributions such as translation, rotation and magnification ("linear residuals") as an indication of target robustness. However, neither TMU nor linear residuals alone or in combination can adequately represent the full complexity involved in determining the optimal target design. Poor selection of the overlay mark can cause issues such as frequent false alarms or even yield loss. As the overlay control specifications become tighter, metrology engineers need a more sophisticated target selection methodology that goes beyond the traditional TMU and residual metrics.

In this paper, the authors employ a source of variance (SOV) methodology which decomposes raw overlay data into various systematic components such as wafer-level, field-level, and un-modeled components. By comparing the SOV component differences among different overlay mark designs and by applying knowledge of lithography and process setup conditions, the metrology engineer can determine the optimal overlay mark to meet production overlay control requirements.

Metrology, Inspection, and Process Control for Microlithography XXV, edited by Christopher J. Raymond,
Proc. of SPIE Vol. 7971, 79712B · © 2011 SPIE · CCC code: 0277-786X/11/$18 · doi: 10.1117/12.879378

2. OVERLAY DECOMPOSITION –SOURCE OF VARIANCE (SOV) ANALYSIS

In production, lithography engineers commonly observe that overlay data can vary significantly for different marks printed in nearby locations, even when processed at the same time. Ideally the overlay data should be identical for targets printed with the same scanner at the same time. When there is an overlay difference between such marks, the cause must be a variation in manufacturing that distorts the geometrical profile of the mark. If lithography patterning is responsible for distortion of the target profile, its contribution to overlay error should be field-level. If the process (etch or CMP) is responsible for distortion of the overlay mark, its contribution should be wafer-level. Therefore, when selecting optimal targets from a pool of candidates, it makes sense to break down the overlay data into different contribution categories.

2.1 Overlay contributors

Ideally, metrology of the overlay mark should reflect the scanner stage stepping accuracy, layer alignment error, and field shot distortion. In addition, as described above, process effects can contribute false overlay error beyond the scanner contributions. Since overlay is determined by taking an image of the overlay mark, the metrology tool's repeatability (precision) and optical imperfection (uncorrected TIS) can also contribute to overlay uncertainty. Finally, mask registration error in today's most advanced process nodes has become a significant contributor and can use up a sizeable portion of the overlay error budget.

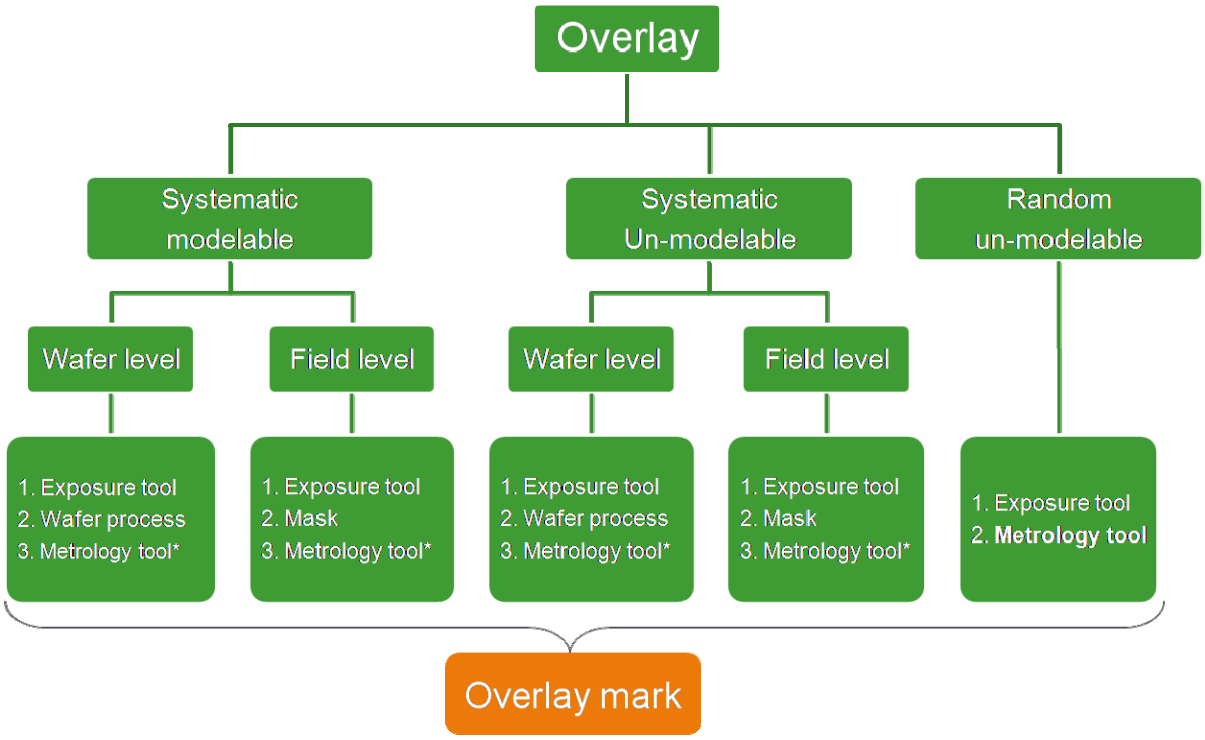

Figure 1. Overlay is decomposed into three major data modeling categories. Each category is further separated by wafer and field level sources of variance that are attributable to the physical contributors.

2.2 Data decomposition

Based on the sources of overlay error, the raw overlay data from several wafers is decomposed into three major categories. The first category includes the "modelable" components, that is, those components which can be expressed

using typical polynomial equations as shown in Eq (2). This category includes overlay contributors from wafer and field levels, both of which are modeled independently.

$$OVL = K_1 + K_2 * x + K_3 * y + K_4 * x^2 + K_5 * xy + K_6 * y^2 + K_7 * x^3 + K_8 * x^2 * y + K_9 * x * y^2 + K_{10} * y^3 + \ldots \quad (2)$$

After removing the systematic, modelable overlay components at both the wafer and field levels, the residual data can be further divided into systematic unmodeled wafer and field level signatures and random un-modelable contributors. Graphic illustrations of the systematic modelable and unmodeled, wafer- and field-level components are shown in Figure 2. After removing the systematic components from the data, the remaining data is assumed to arise from non-systematic, random sources.

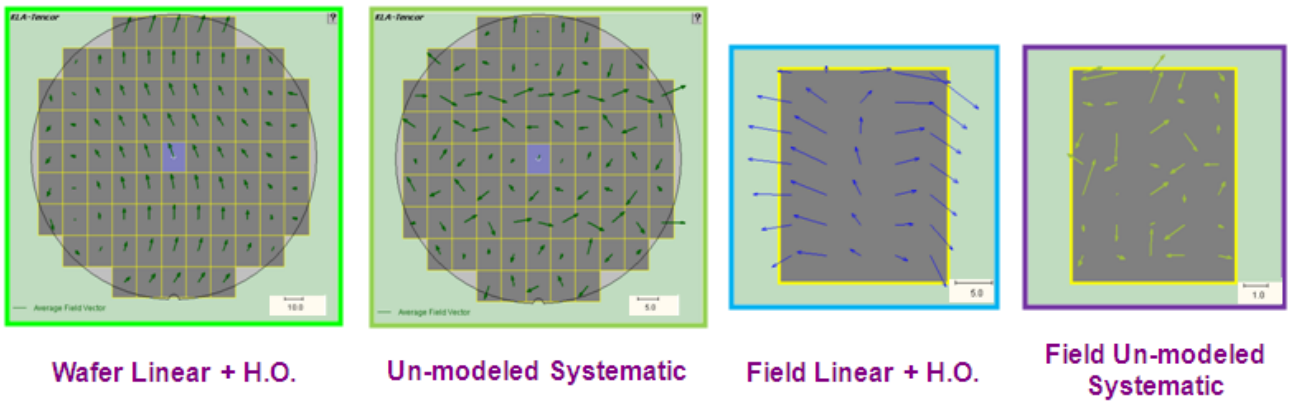

Figure 2. Overlay data is mathematically modeled and sorted into systematic modelable and systematic un-modelable components at the wafer and field levels. Any residual error is assumed to arise from random sources. The decomposed overlay vector plots provide visual aids for overlay troubleshooting

$$OVL\ \sigma^2 = \sigma^2_{\text{wafer modelable}} + \sigma^2_{\text{wafer unmodelable systematic}} + \sigma^2_{\text{Field modelable}} + \sigma^2_{\text{Field unmodelable systematic}} + \sigma^2_{\text{unmodelable random}} \quad (3)$$

Once the data is decomposed, one can create a SOV stack bar plot based on Eq (3). Figure 3 shows an example of overlay raw data decomposition in which the systematic, modelable overlay error is further separated into linear and high order components by K-T Analyzer. To perform such data decomposition, data sampling density has to be sufficient at both the wafer and field levels. For smaller sampling densities, some SOV components cannot be characterized. For instance, a field that contains data from only four points is not sufficient to characterize high order field component errors.

2.3 SOV plot interpretation

The SOV plot is essentially a variance domain based graph which integrates and color-codes the systematic modelable and un-modelable, wafer and field-level overlay error correctables and residual random errors into one single bar plot. Connecting the physical overlay contributors to each of the SOV components can greatly benefit the understanding of performance differences among targets.

While comparing the target performance among various designs, one can simply plot the SOV of each target in a single chart and ascertain which SOV components show the largest differences. If an overlay mark is not compatible with an etching process, for instance, it could induce target profile asymmetry and lead to wafer level overlay error differences between overlay marks. The presence of a field level overlay difference between overlay marks, can imply lithography patterning as the major cause. When there is an unmodeled random component difference, a metrology issue could be

the cause. For instance, a poor contrast target could reduce metrology precision or result in a measurement flyer, and thereby produce a higher unmodeled random component.

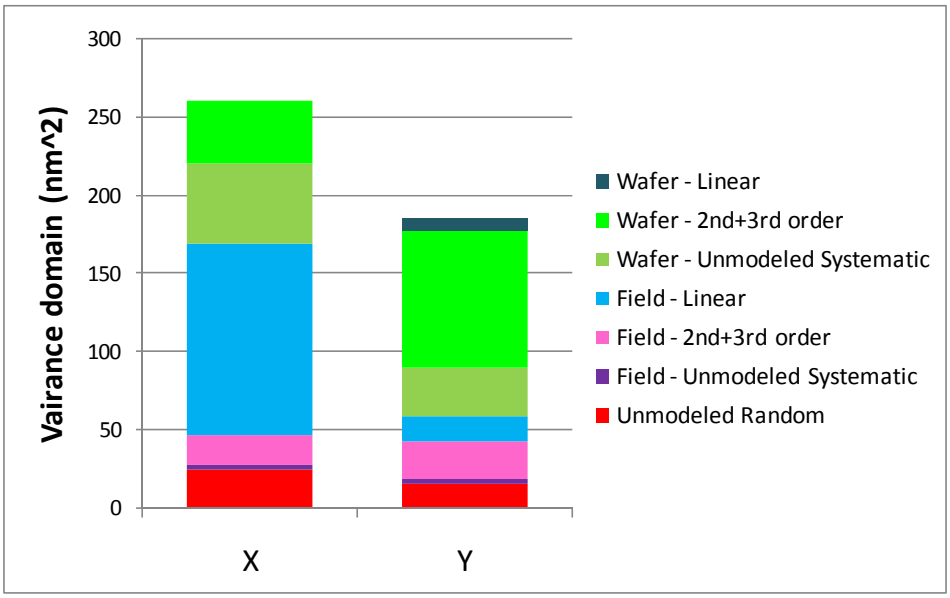

Figure 3. Overlay sources of variance are stacked up and plotted in variance domain. Taking the square root of the variance is equivalent to 3 sigma. From the stacked bar chart, one can easily visualize the major overlay contributors. The bottom red colored component is mainly coming from scanner stage. For different overlay targets printed on the same wafer, a smaller red component means less metrology noise.

3. PROCESS IMPACT ON OVERLAY MARK

Traditional overlay marks usually have feature widths that are significantly larger than the device feature size. The processing steps (etch or CMP) are optimized for the smaller device features. As a result, the overlay mark pattern might not be fully etched out while the device cell is already completely formed. The resulting overlay structure might therefore differ from the ideal symmetrical pattern and introduce false overlay error not representative of the real device overlay error. In this section, we apply the SOV methodology to investigate the impact of the process on overlay error, arising from the difference between the feature size of the overlay mark and that of the device features.

3.1 Process impact identification

An asymmetric target profile will highly influence the results of overlay metrology. A simple experiment was conducted to determine how asymmetry induced by the process affects the overlay metrology result, as shown in Figure 4. In this experiment, overlay error was measured at nine sites across a 300mm wafer. Each site was measured at 11 different focal positions. SOV analysis was then performed on each data set and compared. Each bar in Figure 4 represents the nine-site overlay variance at a certain focal plane. These data indicate that process induced target asymmetry is a linear, wafer-level contributor to overlay error.

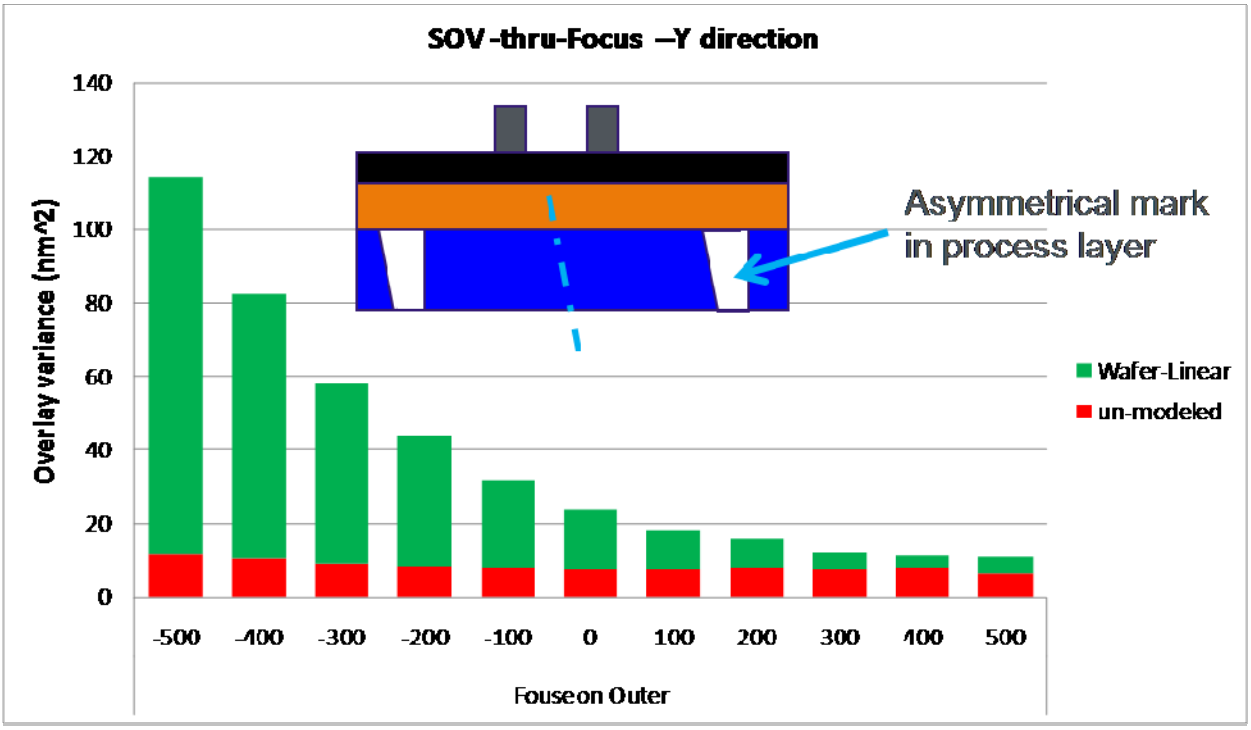

Figure 4. Asymmetric target profiles can induce through-focus dependence to overlay metrology results. The SOV plot indicates process induced target asymmetry is a linear wafer- level contributor to overlay error in our case study.

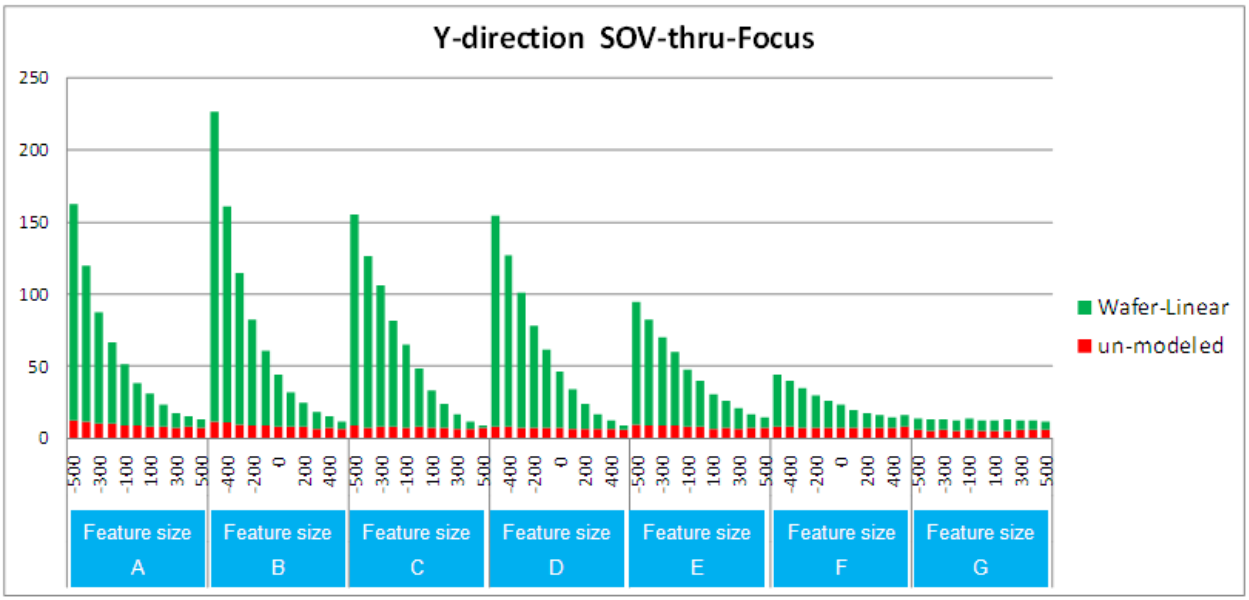

Figure 5. Target asymmetry changes through-focus behavior for overlay metrology. The asymmetry starts to improve when the feature size gets smaller than a certain threshold as shown from the SOV-through-Focus plot.

3.2 Overlay mark feature size

In the next experiment, several overlay marks with features ranging from sub-micron to more than 1μm were laid out next to one another. An overlay through-focus study found that target asymmetry can be correlated to feature size, as shown in the SOV through-focus plot in Figure 5. One can also observe from the SOV plot that the process impact on the target is a linear wafer level effect.

4. LITHOGRAPHY COMPATIBILITY WITH OVERLAY MARK

As segmented targets are expected to have better process compatibility than unsegmented targets, this study included an investigation of how segmentation closer to design rules can improve target patterning compatibility to photolithography illumination conditions. Using different illumination settings for different layers is becoming a more common practice at advanced device nodes. Therefore, for a segmented overlay mark, it is important to consider the scanner illumination setup to make sure the features are printable with the desired profile. The following two sections will discuss lithography compatibility issues and how SOV analysis can be used to help with overlay mark evaluation.

4.1 Overlay mark printability

X-dipole illumination is used for printing vertical (Y) structures in the device. That means overlay target segmentation should be restricted to the Y direction. However, AIM™ targets are typically segmented along the coarse structure. This means that, in the Y-direction, the AIM target will have a horizontally segmented fine feature, which is not optimized for X-dipole illumination. Figure 6a shows an example of an overlay target with the feature size too small to be printed because its segmentation direction is not optimized for X-dipole illumination. Figure 6b shows an example of a target pattern that has collapsed due to an improper duty cycle, even with the feature size above the printability threshold. Therefore, when using an overlay target with a segmented pattern not optimized to the dipole illumination setup, feature size and duty cycle have to be carefully chosen to avoid printability issues.

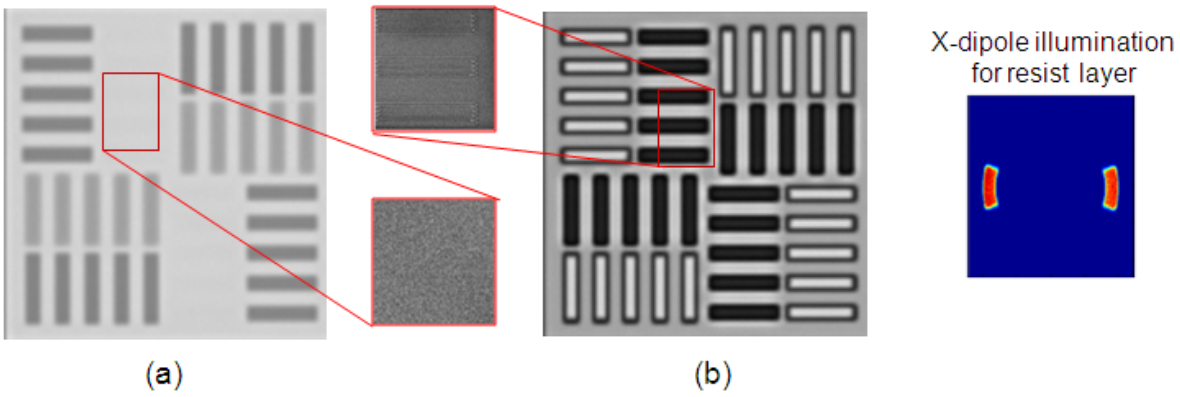

Figure 6. Overlay mark with x-dipole unfriendly segmentation could lead the pattern either (a) to be unprintable, or (b) to collapse when the segmented line width is the wrong size.

4.2 Overlay mark compatibility with illumination and metrology

Even if an overlay mark's segmentation is not an ideal match with the illumination setup, its pattern might still print correctly if the feature size and duty cycle are correctly chosen. However, the possibility of printing a segmented target with uneven line end shortening or poor line end profile must still be considered. To investigate the uneven line end shortening effect, the authors intentionally designed targets which were completely incompatible with X-dipole illumination. Figure 7 shows such an AIM target: the resist layer (the rectangle covered) was horizontally segmented in both X and Y. Since the segmented feature size is above the printability threshold, the AIM mark was still formed.

However, after careful examination of the line end profile, it is clear that the quality is compromised. The line end quality degrades the edge that is used for overlay calculation and therefore decreases the reliability of the measurement.

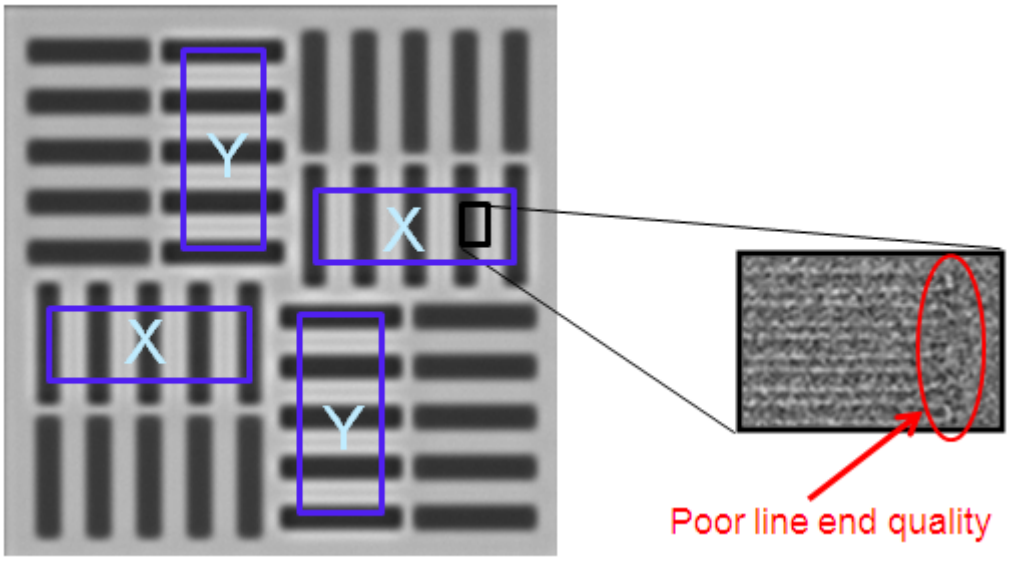

Figure 7. The coarse bars in both the X- and Y-kernel areas are horizontally segmented, which is incompatible with X-dipole illumination. Even though the mark pattern can be printed, poor line end quality might result in an incorrect target profile. Including wrong edge profiles in the metrology information in X-direction will compromise the reliability of the X-overlay data.

By using SOV methodology as shown in Figure 8, two distinct groups of overlay marks with significant field level overlay error component differences can be observed. The major difference between the two groups arose from the segmentation layout. Targets S1 to S6 are segmented to be illumination-friendly, which results in small and similar field level overlay errors. In contrast, targets S7 to S16 with segmentation unfriendly to the illumination setup (similar to Figure 7) produce a huge field level overlay error component and their values are inconsistent from target to target. With knowledge of the target design and scanner illumination setup, it is not a surprise that the overlay error results from those marks are unreliable in the X-direction.

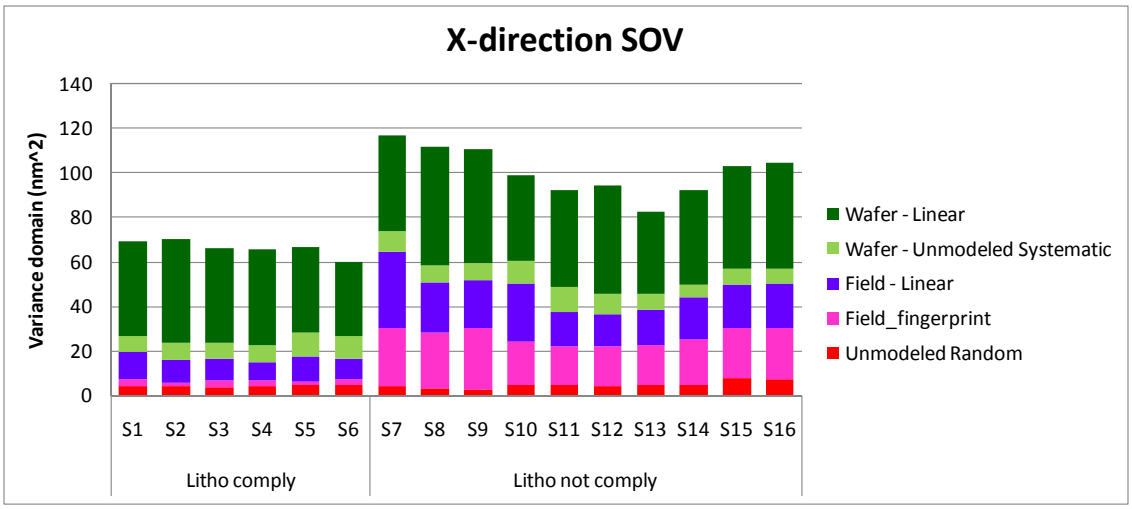

Figure 8. Litho-unfriendly overlay marks (S7-S16) result in exaggerated overlay error, as their field level contributions were significantly different from those of the litho-friendly overlay marks (S1 to S6). For certain targets (S15 & S16), the random noise level also was higher than that of the others.

5. SUMMARY

Traditional metrics used for overlay target selection, such as TMU and/or residual error, may not be sufficient to fully understand and gauge the merits of different target designs for advanced design rules. A new approach using source of variance (SOV) analysis, as provided by K-T Analyzer, has been shown to be a more comprehensive methodology for target performance selection. Using this new approach, we can better minimize costs associated with reticle redesigns and/or process changes in order to meet the metrology requirements of the most advanced processes as well as optimize metrology performance in the shortest amount of time.

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