# Simulation of Non-Uniform Wafer Geometry and Thin Film Residual Stress on Overlay Errors

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## ABSTRACT

The deposition of residually stressed films in semiconductor manufacturing processes introduces elastic distortions in the wafer that can contribute to overlay errors in lithographic patterning. The distortion induced by film deposition causes out-of-plane distortion (i.e. wafer shape) that can be measured with commercial metrology tools as well as in-plane distortion that leads to overlay errors. In the present work, overlay errors and out-of-plane distortion of wafers resulting from residual stresses that are non-uniform over the area of wafer are examined using computational mechanics modeling. The results of these simulations are used to examine the correlations between wafer shape features and overlay errors. Specifically, connections between overlay errors and metrics based on the slope of the wafer shape are assessed.

**Keywords:** overlay, residual stress, wafer shape

## 1. INTRODUCTION

Controlling overlay errors in lithographic patterning is currently and will continue to be a challenge in semiconductor manufacturing.[1] There are multiple sources of overlay error[2] and minimizing the contribution from all sources is essential to meet the tight overlay budgets at advanced nodes. One of the sources of overlay error is wafer geometry. Wafer geometry components span over a wide range of spatial frequency and some of the key geometrical characteristics are shape (a lower frequency surface variation of the wafer), flatness or thickness variation of the wafer, Nanotopography (higher frequency surface variations of the wafer with a spatial wavelength of 0.2-20 mm and height of few nm), roughness (spatial wavelength in the order of microns and height of few A°), edge roll-off, and edge dimension/profiles (see Fig. 1). These wafer geometry features may be a result of the wafer manufacturing processes (e.g., sawing, grinding, polishing) or, in some cases, can be imparted through the deposition of residually stressed films.

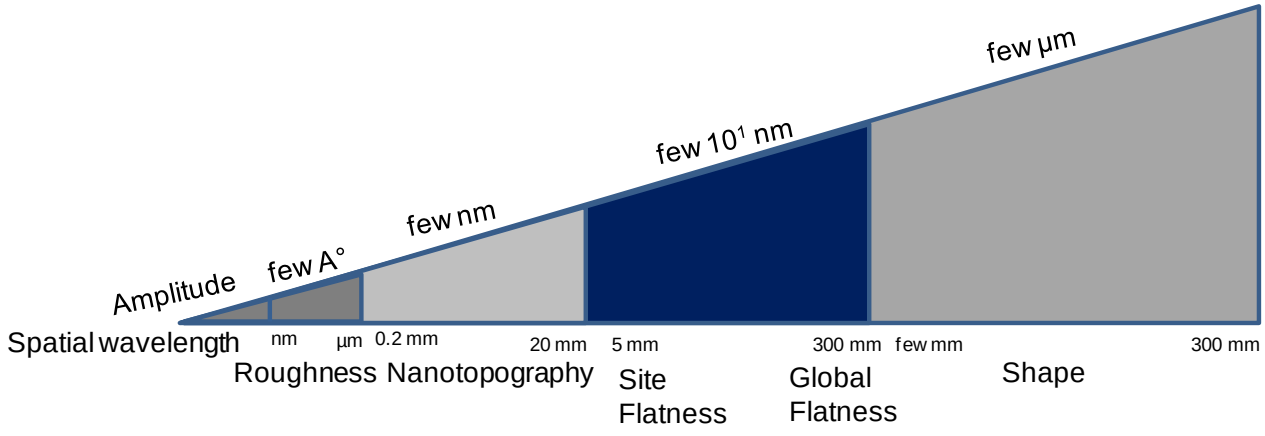


Figure 1. Summary of range of wafer geometry parameters.

Metrology, Inspection, and Process Control for Microlithography XXV, edited by Christopher J. Raymond,
Proc. of SPIE Vol. 7971, 79711U · © 2011 SPIE · CCC code: 0277-786X/11/$18 · doi: 10.1117/12.879493

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The deposition of residually stressed thin films, which is common in semiconductor processing, elastically deforms the wafer and causes both in-plane and out-of-plane distortion of the wafer. The distortion of the wafer can result in overlay errors that cannot be corrected with current scanners. In the present work, the relationship between overlay errors, out-of-plane distortion of the wafer, and residual stress is examined using computational mechanics modeling. The goal of the present study is to investigate the relationship between out-of-plane distortion, which can be measured using commercial metrology tools, and overlay errors in order to establish new approaches to monitor and manage overlay. Here, we specifically focus connections between overlay errors and metrics based on the slope of the wafer shape.

## 2. MODELING AND METHODS

Overlay is the relative misalignment between two lithographic patterning steps. Here, we consider a simplified process consisting of two patterning steps and one film deposition step, as shown in Fig. 2. In step A, a wafer is patterned; two representative features separated by distance $L$ are considered to illustrate overlay. In step B, a film with residual stress is deposited and elastically deforms the wafer. This leads to in-plane distortion (IPD) that changes the distance between the features on the wafer surface ($\Delta L$ in Fig. 2) as well as out-of-plane distortion (OPD) that results in a shape change of the wafer. In step C, the wafer is chucked in the lithography tool and the second layer is patterned. When the wafer is chucked, the OPD of the wafer is largely removed and the features on the pattern surface shift due to the deformation induced by chucking. The deformation induced by chucking, $\Delta L_C$, generally offsets a portion of the distortion induced by the film deposition but not completely (i.e., $\Delta L$ and $\Delta L_C$ have opposite signs, but are not equal in magnitude). The difference in position between the two features ($\Delta L+\Delta L_C$) leads to overlay errors. Lithography tools allow for some corrections to be made, thus the overlay error is the residual of $\Delta L+\Delta L_C$ after the correction is applied.

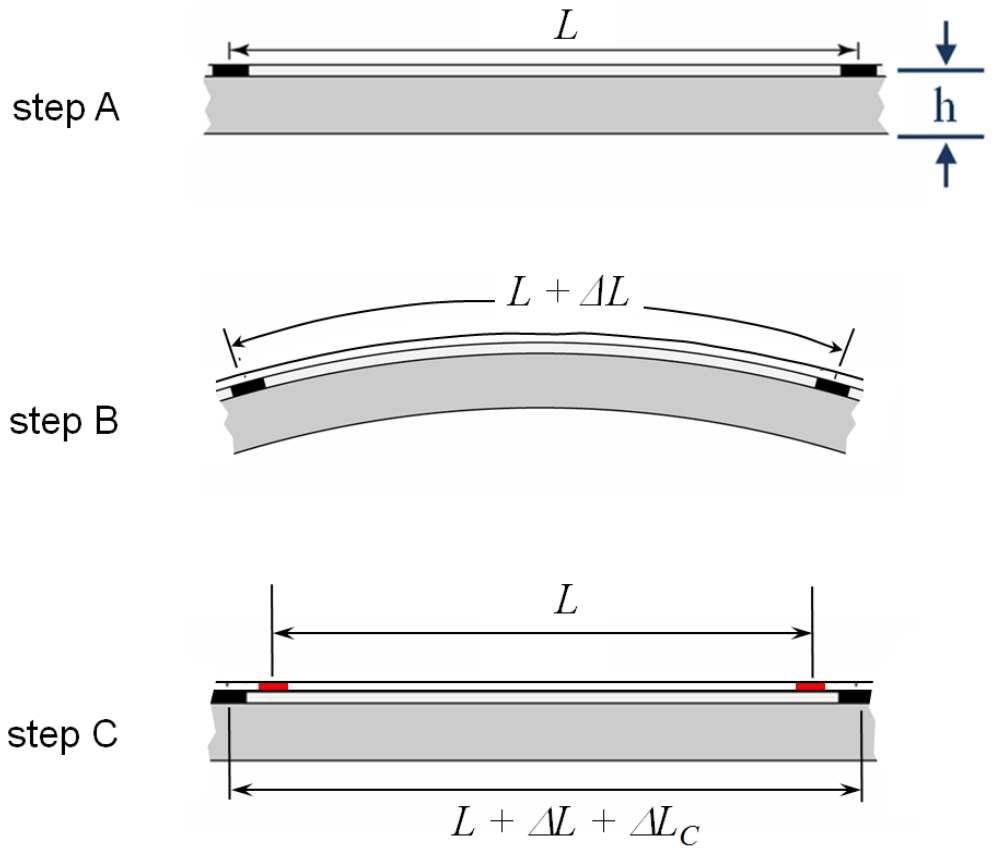


Figure 2. Schematic of overlay error between patterning steps in step A and step C resulting from the deposition of a residually stressed film in step B.

A three-dimensional finite element model that simulates the three step process shown in Fig. 2 has been developed in order to investigate the relationship between film stress, wafer shape, and overlay error. The model is summarized in Fig. 3 and will be described in detail elsewhere[3]. In the first step of the model, the distortion due to the deposition of a residually stressed film is simulated. The OPD and IPD are calculated based on the wafer and film geometry, elastic properties, and residual stress in the film. The spatial distribution of residual stress in the film is described by the function given in Fig. 3, where the six coefficients, $s_{01}$ through $s_{06}$, are chosen to achieve different stress fields. In the second step, the chucking of the wafer is simulated. The total in-plane distortion from steps 1 and 2 is calculated and linear overlay corrections, as listed in Fig. 3 are applied. From this set of models, the shape of the wafer after film deposition and the overlay errors across the wafer are calculated. The overall wafer shape and the residual wafer shape after removing a second-order fit are both reported.

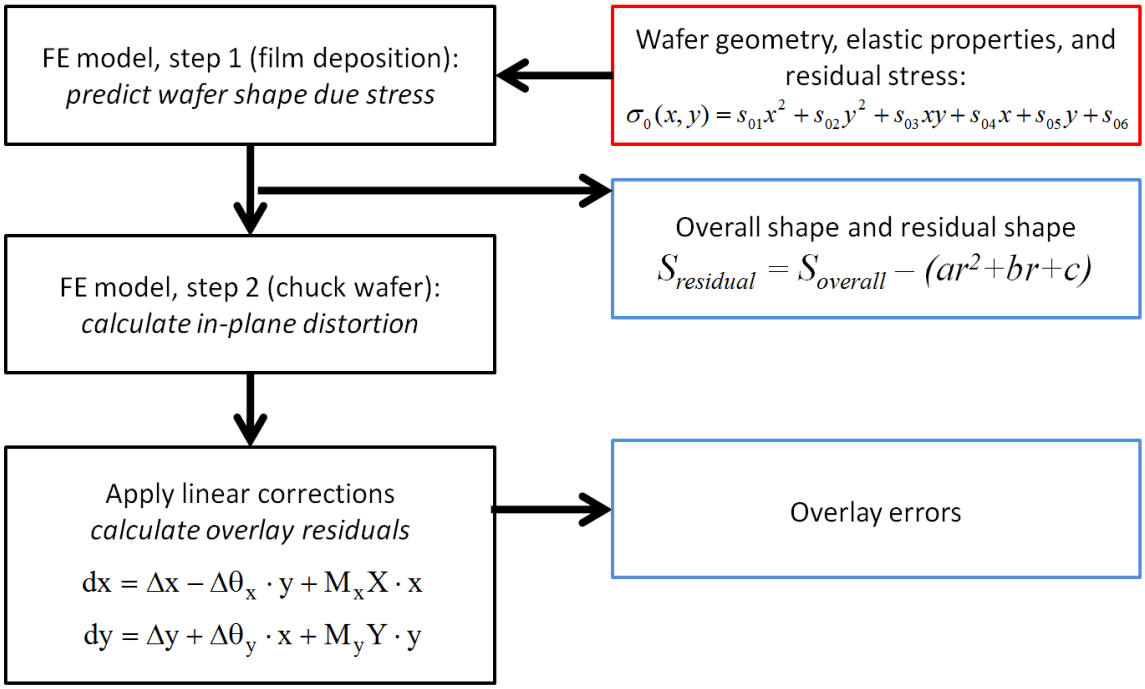


Figure 3. Summary of the computational model used to predict overly error and wafer shape resulting from the deposition of residually stressed thin films.

For all simulations reported here, the wafer is 775 μm thick, 300 mm in diameter, and is modeled with the elastic properties of silicon, Young's modulus of elasticity E=150 GPa and Poisson's ratio ν=0.2. The film is 0.5 μm thick and results for six different residual stress distributions are reported (Fig. 4, left column). For the overlay calculations, the dimensions of lithography fields were assumed to be 12.16 mm (x) by 14.16 mm (y).

To study the impact of wafer geometry on overlay errors, overlay errors are correlated with global and local geometry metrics. From previous work[3,4], it was observed that local wafer shape variations correlated well with overlay errors across the wafer. To capture local wafer shape variations a derivative of wafer shape at each data point is computed using the neighboring pixels to obtain the slope map of wafer shape. At each pixel, slope in the x-direction and slope in the y-direction are computed, and a radial slope at that pixel is computed from the x- and y-slope and the spatial location of the pixel with respect to the center of the wafer (wafer coordinate system). To study the impact of global wafer shape due to non-uniform thin film residual stress on overlay errors, the maximum slope of the wafer was computed. To do a correlation of local metrics and overlay errors in a site/field, the peak-to-valley of shape slope at the site/field of interest is computed. In this paper, four sites at different spatial locations on the wafer surface are chosen to correlate to average radial overlay per field.

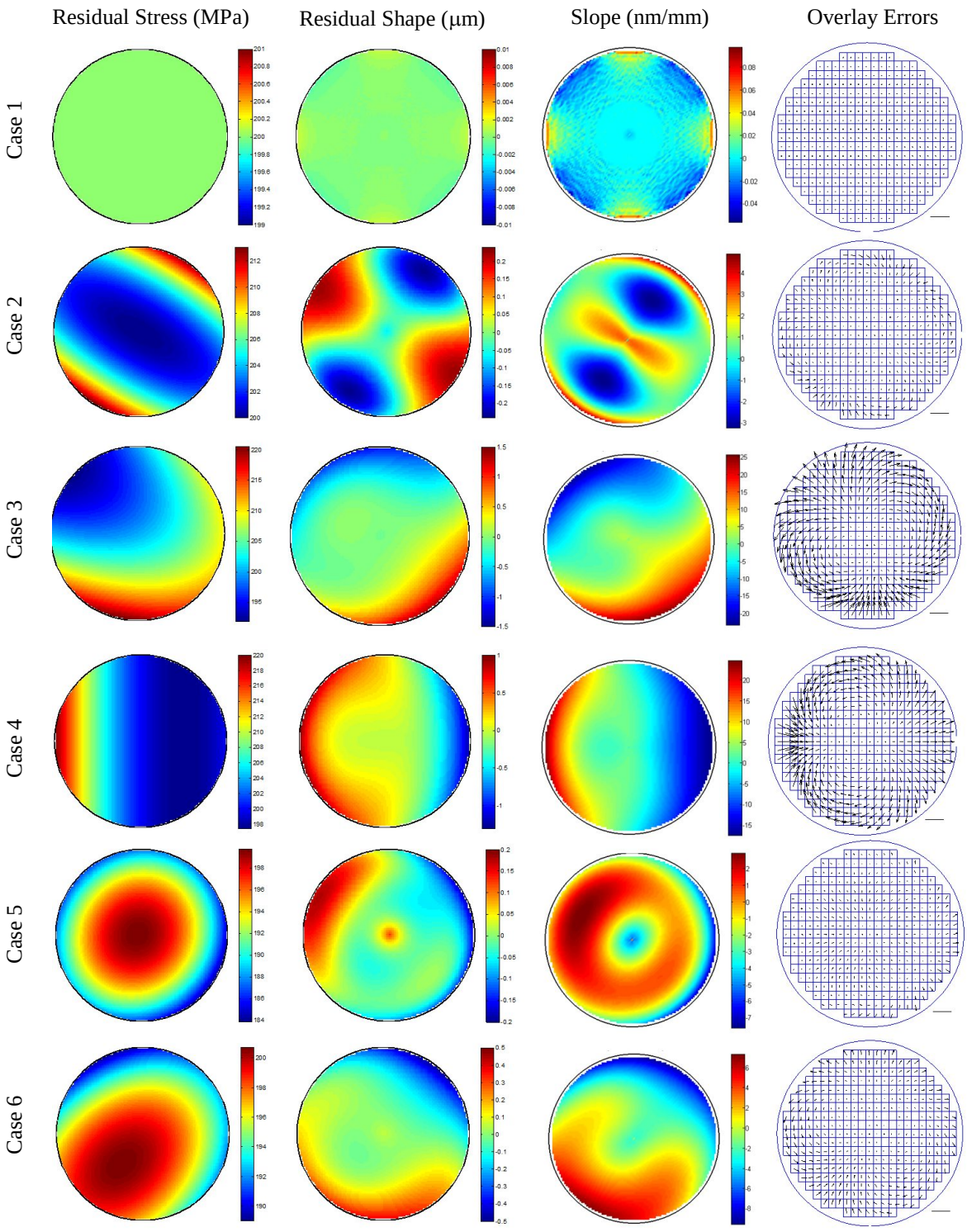


Figure 4. Summary of six cases examined showing residual stress distribution, residual shape, local slope, and overlay errors. In the overlay vector maps, the scale bar in lower right is 3 nm in length.

## 3. RESULTS AND DISCUSSION

The residual stress distributions, residual shape, local slope, and overlay errors for the six cases examined are summarized in Fig. 4. All of the stress distributions considered have a nominal residual stress of 200 MPa and the variation in stress across the wafer is less than 10% of this nominal stress in all cases. As shown in Fig. 4, case 1 has a uniform stress and cases 2-6 have a range of different stress distributions. The overall shape for each wafer is not shown here because for all cases the overall wafer shape looks approximately parabolic as the nominal stress of 200 MPa is much larger than the variation of the residual stress. The differences in shape among the six cases only become evident when a second order fit to the shape is removed and the residual shape is plotted (column 2 in Fig. 4). It is important to realize that higher-order shape features introduced by nonuniform residual stresses are usually only observable when the macroscale curvature of the wafer is removed by removing a second order fit from the shape map. Once the second order fit is removed, the magnitude of residual shape is observed to correlate with stress non-uniformity and, in general, higher stress non-uniformity leads to higher residual shape (Fig. 4). The local slope of the residual shape and overlay errors for each case are shown in the third and fourth columns of Fig. 4, respectively. From the results, it is observed that regions with large residual shape and slope generally have larger overlay errors. Note that the scales of the surface plots in Figure 4 vary from wafer to wafer,.

To explore the relationship between overlay error and slope, the correlation between the maximum overlay error and maximum slope in the x- and y-directions for each of the six cases is shown in Fig. 5. Overall, there is a strong correlation between the maximum slope and maximum overlay error for the six cases examined here. In addition, a site shape slope metric was calculated for four sites across each wafer and the correlation between site shape slope peak-to-valley and an average radial overlay error in the corresponding site was examined (Fig. 6). As shown in Fig. 6, there is a positive correlation between site shape slope and overlay error, but the $R^2$ value is only 0.652. The scatter and lower $R^2$ value is due to the fact that the site shape slope quantity is essentially a peak-to-valley of slope value for the site, while the average radial overlay per site is the average error at a specific site/field.

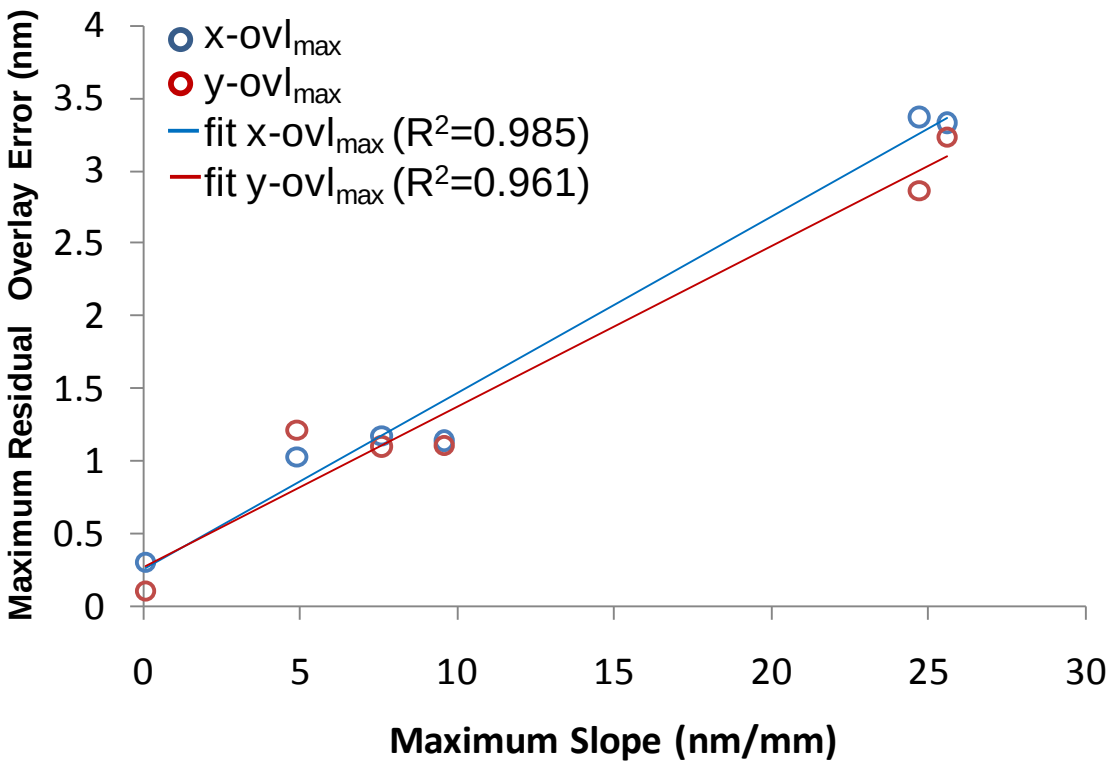


Figure 5. Correlation between the maximum overlay error and maximum slope for each of the six cases investigated.

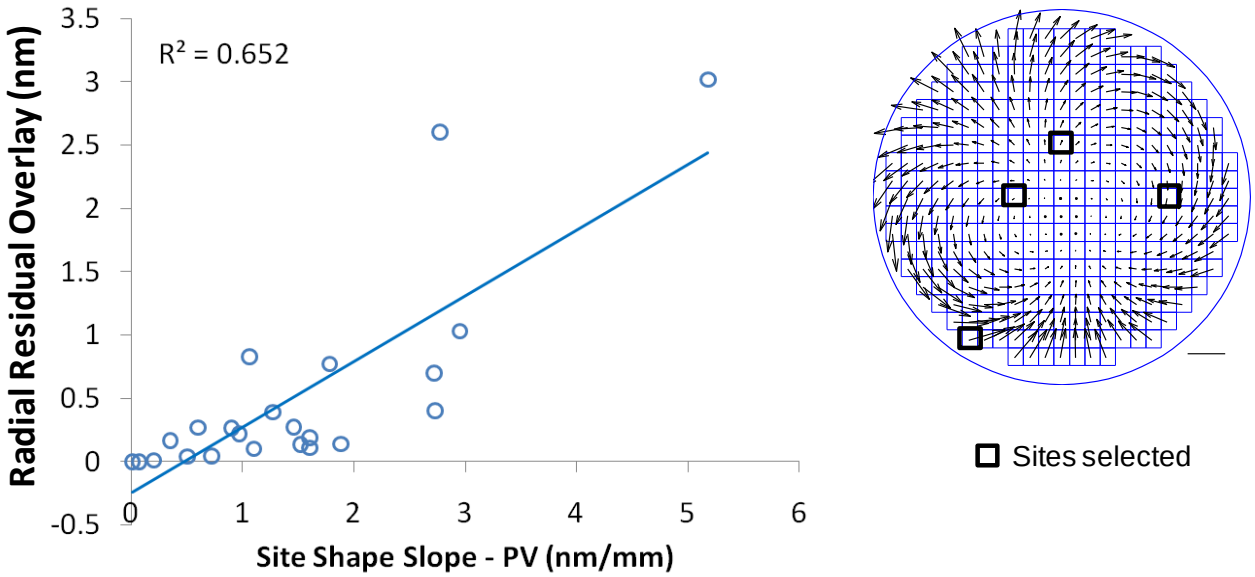


Figure 6. Correlation between site shape slope and overlay error for 4 sites on each of the six wafers.

These preliminary correlations reported here demonstrate the connection between non-uniform residual stress, local wafer geometry metrics, and overlay error. Further investigation, both modeling and experiment, is required to firmly establish the realtionship observed here. However, the present analysis clearly illustrates the underlying mechanics of one source of overlay error and its relationship to wafer geometry.

## 4. SUMMARY

Computational mechanics modeling has been used to examine fundamental connections between overlay errors, wafer shape, and residual stresses. In general, non-uniform residual stresses lead to local shape variations and overlay errors. The results show that features in the shape data, in both the height and slope domain, are related to overlay errors. This suggests that shape measurements may allow for identification of wafers that are likely to have large overlay errors and may lead to new approaches to managing overlay.

## REFERENCES

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