

Impact of mask line roughness in EUV lithography

Alessandro Vaglio Pret^{a,b}, Roel Gronheid^a, Trey Graves^c, Mark D. Smith^c, John Biafore^c

^aIMEC, Kapeldreef 75, B-3001 Leuven, Belgium

^bKatholieke Universiteit Leuven (K.U.Leuven), department of Electrical Engineering (ESAT),
Kasteelpark Arenberg 10, B-3001, Heverlee (Belgium)

^cKLA-Tencor - Finle Division Austin, TX 78759

vaglio@imec.be

ABSTRACT

Resist line edge/width roughness is one of the most critical aspects in EUV lithography for the 32 nm technological node and below. It is originated by the uncertainties which characterize the lithographic process: source speckle effect, mask line and surface roughness, mirror roughness, flare effect and resist pattern formation all contribute to the final roughness.

In this paper mask and resist line edge roughness were compared by means of frequency analysis on top-down SEM images: it was found that low frequencies mask roughness are well correlated with the Power Spectral Density of the resist roughness. Mask high frequencies components resulted less critical due to the natural cut-off of the optical system.

Experimental data for both mask and resist were implemented in the PROLITH Stochastic Resist Model simulator to quantify the mask line edge roughness contribution to the final resist roughness: the results showed that 16% of the low frequency resist roughness component is originated at the mask level. For that reason, mask impact was set as 0.6 nm of the overall line edge roughness resist budget.

Keywords: EUV Lithography, line edge/width roughness, power spectral density, optical system cut-off

INTRODUCTION

Resist platforms for Extreme UV (EUV) Lithography have not yet reached the ITRS¹ target for Line Edge/Width Roughness (LER, LWR) for 32 nm technological node and below. In fact, resist roughness is one of the major issues which still shadow the EUVL entrance in a future high production volume regime.

Resist LER in EUVL arises from many contributions, one of those is the mask roughness itself. Previous experimental studies² and simulations³ have shown that both mask surface and mask absorber roughness have a not negligible impact on the final printed pattern. However, in literature it was not found a quantitative evaluation of mask LER (LER_M) contribution to resist roughness.

In this paper, experimental analyses of both mask and resist LER were matched with stochastic simulations performed by PROLITH Stochastic Resist Model (version X.3.2) software⁴. Comparing simulation and experimental results, it was possible to identify and quantify the LER_M contribution to resist for 36 nm half-pitch structures.

In the first paragraph, roughness analysis of both EUV mask and resist are presented, mainly focused on Critical Dimension-Scanning Electron Microscopy (CD-SEM) top-down images and Power Spectrum Density (PSD) analysis^{5,6}. In the second paragraph, experimental results of resist and mask are compared. The third paragraph is dedicated to the simulation setting: resist modeling, PSD analysis of simulated resist, and mask contour-plot injection in PROLITH are reported. In last paragraphs, simulated and experimental results are compared, stressing the Low Frequency (LF) roughness importance in resist performance evaluation.

METROLOGY SETTING

For this experiment, 36 nm half pitch (@ 1X) line and space structure was exposed. A EUV Mo/Si multilayer mask with Ru capping layer and TaBN/TaBON absorber was used. The exposures were performed with the ASML Alpha Demo Tool installed at IMEC, with $\lambda = 13.5$ nm and a conventional illuminator with NA = 0.25 and $\sigma = 0.5$. SEVR-59 resist

with 65 nm thickness on Silicon was selected for its good performance in terms of resolution, LER and sensitivity⁷. The dose to size for 36 nm line CD was 17.5 mJ/cm².

To evaluate both resist LER and LER_M, top-down CD-SEM was used for image capturing (Figure 1), while the analyses were performed by the off-line software LERDEMO⁸. In order to match the CD-SEM metrology between mask and resist evaluations, a Field of View (FoV) of ~ 0.7 x 0.7 μm² with pixel sizes of ~ 5 nm was set in the direction along the lines. In x direction (perpendicular to the lines), a smaller pixel size (~ 1 nm) was chosen to have a better resolution along the resist protrusion. For the sake of simplicity, all the dimensions are normalized @ 1X.

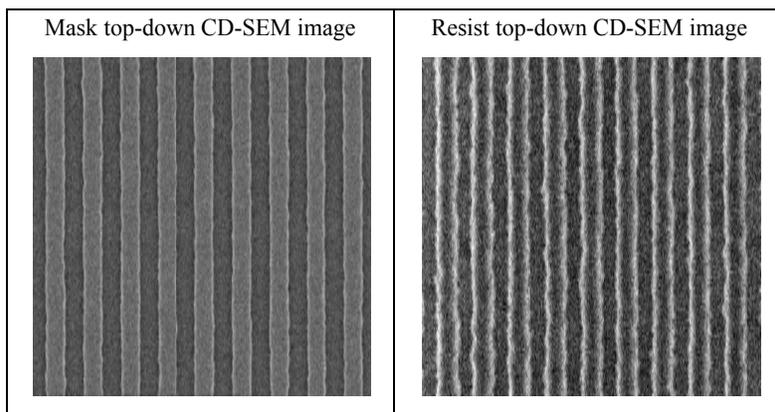


Figure 1: 36 nm half pitch top-down CD-SEM images for EUV mask (left) and resist (right). After metrology match, both FoV correspond to a square-scan of ~ 0.7 x 0.7 μm² dimension (@ 1X) with rectangular pixel sizes of ~ 1 nm in x-direction (perpendicular to the lines) and 5 nm in y-direction (along the lines).

To perform a statistical analysis, 23 resist images (~ 140 lines) were taken⁹, meanwhile only 3 CD-SEM mask images were captured (~ 30 lines), due to analysis limitations. Image averaging was necessary to reduce the noise, in particular in the LF roughness region of the PSD.

EXPERIMENTAL RESULTS

Mask vs. Resist LER

In Table 1, CD, CD Uniformity (CDU) and 3σLER for resist and mask are reported: all of them were evaluated on 0.7 μm line length. 3σLER_{l,r} represents the average of left and right edge. With the used metrology, 3σLER uncertainty is less than 0.15 nm⁹.

	CD (nm)	CDU (nm)	3σLER _{l,r} (nm)
Resist	39.9	1.0	3.6
Mask	36.3	0.7	2.3

Table 1: top-down HITACHI CD-SEM analysis for resist and mask on 36 nm half pitch structure.

In Figure 2, mask and resist PSD (respectively grey and black line) extracted by CD-SEM images are reported. Mask PSD normalization was necessary to overcome the different CD-SEM metrology (magnification, pixel sizes, pixel number) used for resist image capturing. The two PSDs appear to be similar in the low and mid frequency range, while for $f > 20 \mu\text{m}^{-1}$ they tend to deviate.

Considering the optical system cut-off, it is easy to explain why mask High Frequency (HF) roughness is relatively higher than on wafer: mask pattern is defined by electron-beam lithography, a process without any optical cut-off, and thus a more white-noise behavior of the final PSD is generally expected. Then, resist response and mask etch processes contribute to lower mid and high frequency roughness, resulting in the grey PSD plotted in Figure 2. When the mask is used in an optical lithography process, the pattern formation on wafer is modified by an incomplete optical

reconstruction of the mask image. Therefore, during the exposure, several frequency cut-offs occur due to the finiteness of the optical component. The two that mostly affect the aerial image formations, with conventional illumination, are

1st diffraction orders deformation: $f_{min} = \frac{NA*(1-\sigma)}{\lambda} \simeq 9.3 \mu m^{-1}$

when the 1st diffraction orders start falling outside the pupil. It represents the lowest mask frequency transmitted into the resist for which the aerial image is fully modulated by the 1st diffraction orders.

Maximum frequency transmitted by the optical system: $f_{MAX} = \frac{NA*(1+\sigma)}{\lambda} \simeq 27.8 \mu m^{-1}$

when the 1st diffraction order is entirely outside the pupil. It represents the highest mask frequency that can be transmitted into the resist. The inverse of the f_{MAX} gives the minimum printable pitch.

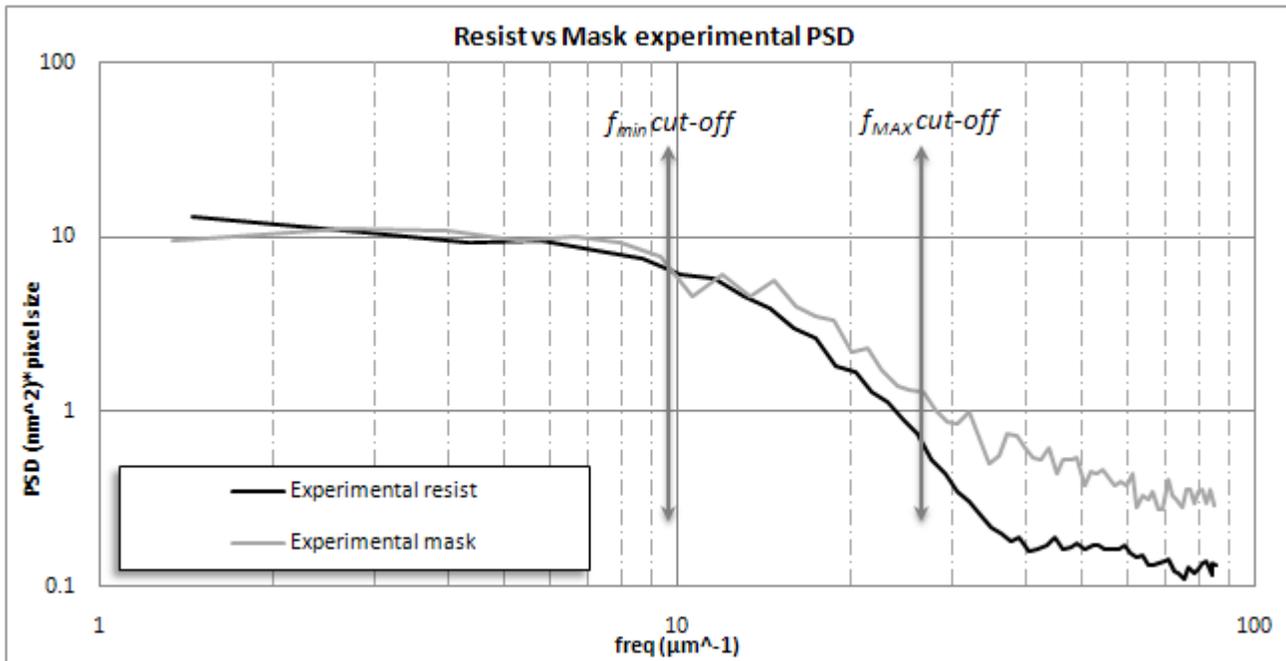


Figure 2: averaged PSDs of top-down CD-SEM images for mask and resist (grey and black line). The two vertical arrows represents the cut-offs of the EUV optical system: f_{min} and f_{MAX} .

Only mask frequency lower than f_{min} are well transmitted into the resist, meanwhile $f > f_{MAX}$ are completely cut-off by the optical system itself. Hence, a natural roughness mitigation effect from mask to resist in the HF region is expected.

For $f > 40 \mu m^{-1}$ (25 nm on wafer), CD-SEM noise flatten the curves, prevailing on LER.

SIMULATIONS RESULTS

Ideal vs. real mask exposures

To evaluate which is the LER_M impact on resist, simulations with ideal and real mask line/spaces contour plot were compared. PROLITH Stochastic Resist Model was used to quantify the mask line roughness impact on resist.

Firstly, the simulator was set in order to reproduce the experimental results (Table 1, first line), proceeding with the same metrology used for the real exposures. Resist modeling, exposure conditions, number of analyzed lines, and real mask contour plot extracted by CD-SEM images (Figure 1, left) were accurately reproduced to match the simulated results (Table 2) with the results obtained on Silicon. CD, CDU and $3\sigma LER$ values were fairly reproduced by the stochastic simulator.

	Real mask stochastic simulation		Ideal mask stochastic simulation		
	Aerial image contrast (average along 0.7 μm lines)	Aerial image NILS (average along 0.7 μm lines)	CD (nm)	CDU (nm)	3σLER _{1,r} (nm)
Simulated resist with real mask	0.86	3.98	38.9	0.8	3.7
Simulated resist with ideal mask	0.86	3.96	38.9	0.6	3.1

Table 2: top: 36 nm half pitch PROLITH Stochastic Resist Model simulations with real (left) and ideal (right) mask contour plot. Bottom: averaged simulated results on 36 nm half pitch structure. Simulations were run with both real and ideal mask contour plot.

Secondly, the same simulations were re-run with an ideal mask contour plot without any roughness (Table 2, last line): resist lines simulated with real mask contour plot showed higher LER, and in some cases μbridging formation, absent in the simulations with ideal mask. After averaging ~ 140 simulated lines, 16% LER difference was found between the two set of simulations. LF mask roughness may explain the CDU difference, too.

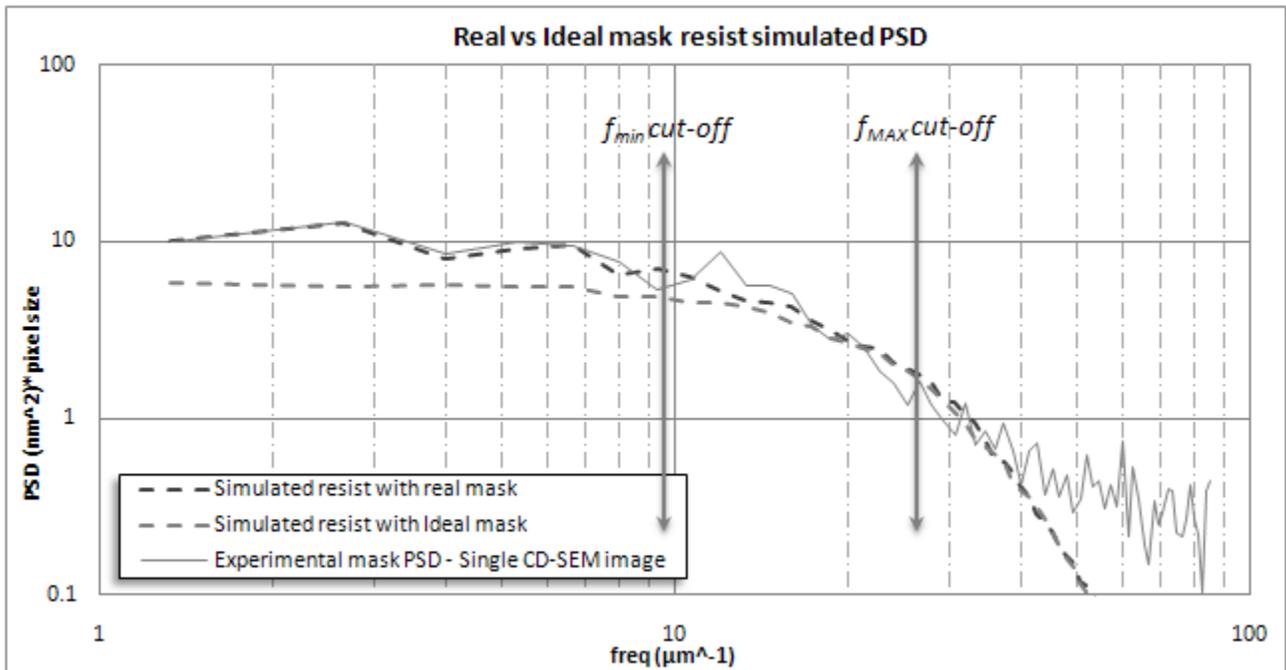


Figure 3: averaged PSDs of simulated resist with real ideal mask contour plot (dotted dark grey- and light-grey line). The solid grey line corresponds to the PSD of the CD-SEM image of the mask used for the simulation (Figure 1, left).

Thirdly, PSDs of the simulated resists with real and ideal mask contour plot were compared (Figure 3). It is clearly visible that the 16% LER difference between real and ideal mask simulation, respectively in dotted dark- and light-grey lines, falls in the LF region, before f_{min} . Due to the equal aerial image quality in terms of Contrast and NILS (Table 2), the observed difference is entirely caused by LER_M . PSD differences were found till f_{MAX} , after that the mask roughness frequencies are completely cut-off by the optical system.

At last, the PSD of the mask CD-SEM image used in the simulation (Figure 1, left) is plotted in the same graph (solid grey line): simulated resist with real mask contour plot PSD and the PSD of the mask image overlap perfectly in the LF region. The PSD superimposition is evident till the 1st diffraction order starts falling outside the pupil ($f \geq f_{min}$). This overlap disappears gradually moving towards higher frequencies till f_{MAX} . This demonstrates that before f_{MAX} , LER_M is highly transferred to the wafer in EUV systems.

It is useful to point out that a longer mask FoV (line length $> 0.7\mu\text{m}$) would allow for the detection of lower mask frequencies ($f < 1.4 \mu\text{m}^{-1}$, the first frequency analyzed in the PSD spectra), with higher impact on resist LER. The lower the considered mask frequency, the more consistent the image reconstruction through the optical system will be.

RESULTS AND DISCUSSIONS

MASK LER_M impact on EUV resist

In Figure 4 the PSDs of Figure 2 and Figure 3 are compared in the same graph. Three main effects are observed:

- the only curve that underestimate LF roughness is the PSD obtained simulating the resist roughness with the ideal mask (dotted light-grey line). On the opposite, simulated resist with real mask (dotted dark-grey line) is well in line with the experimental PSD curve (solid black and grey lines).
- for $f > 40 \mu\text{m}^{-1}$ simulated PSDs rapidly drop (dotted curves), due to the absence of CD-SEM metrology noise.
- for $12 \mu\text{m}^{-1} < f < 40 \mu\text{m}^{-1}$ both the simulated PSDs overestimate the experimental resist PSD. Further investigations are required to establish the origin of this effect.

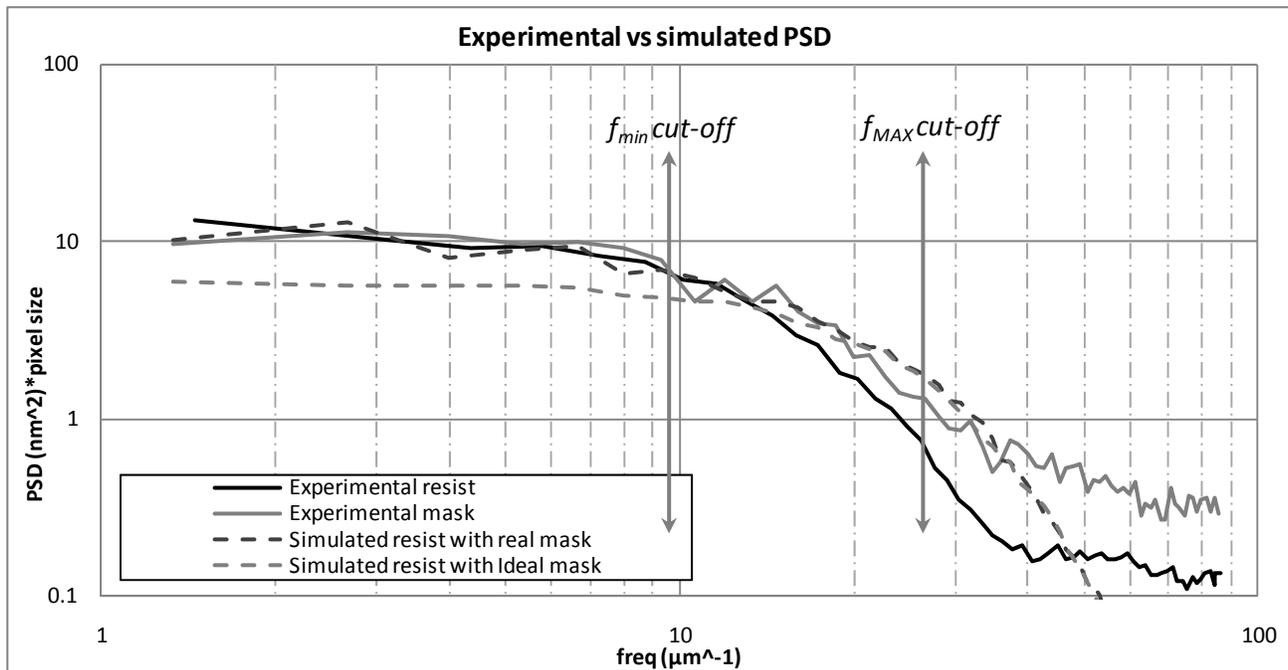


Figure 4: averaged PSDs of top-down CD-SEM images for mask and resist (solid grey and black line). The two dotted curves represent the averaged PSDs of simulated resist with real and ideal mask contour plot (dark- and light-grey line).

For PSD comparison, it was calculated that the 16% LER difference between the simulations with real and ideal mask would correspond to 0.6 nm LER (roughly 1 nm LWR considering uncorrelated lines) in experimental exposures. The mask roughness impact would be mainly in the LF region, where no one of the known smoothing techniques showed any improvement¹⁰.

CONCLUSIONS

In order to quantify mask line edge roughness impact on resist performance in EUV lithography, experimental results have been bridged with stochastic simulation for 36 nm half-pitch exposure.

With the implementation of real mask CD-SEM image contour plot in PROLITH Stochastic Resist Model (Table 2), it was possible to evaluate how the mask absorber roughness is transmitted into the resist. It was found that resist LER decreases by 16% if an ideal mask is used in the simulation instead of a real mask contour plot. Roughness reduction was mainly noticed in the low frequency region, particularly detrimental for inter-transistor performance¹¹, CDU and overlay budget. Moreover, roughness frequencies in this range are hardly improved by any known smoothing technique¹⁰.

Through a comparison of experimental and simulated PSDs for both mask and resist, it was possible to quantify that the mask low frequency roughness impact would be 0.6 nm of the overall resist LER budget (roughly 1 nm LWR).

To keep pace with the Moore's law, resists with lower intrinsic roughness, and optical systems with higher frequency cut-off will be needed. In this scenario, mask roughness will represent a growing segment of the resist roughness specification.

ACKNOWLEDGEMENT

The authors thank Gian Franco Lorusso (IMEC) for the help in metrology matching, Matthew Lamantia (Toppan) for the mask CD-SEM pictures, and Konstantinos Garidis (KTH) for his support with Prolith simulations.

REFERENCES

¹ <http://www.itrs.net/>

² Vaglio Pret, A., Gronheid, R., "Mask line roughness contribution in EUV lithography", *Microelectronic Engineering*, in publication (2010)

³ Naulleau, P. P., Gallatin, G. M., "Spatial scaling metrics of mask-induced line-edge roughness", *J. of Vacuum Science & Technology B: Microelectronics and Nanometer Structures*, vol. 26, issue 6, pp. 1903 – 1910 (2008)

⁴ Biafore, J. J., Smith, M. D., Blankenship, D., Robertson, S. A., van Setten, E., Wallow, T., Deng, Y., Naulleau, P. P., "Resist pattern prediction at EUV", *Proc. SPIE 7636*, 76360R (2010)

⁵ Naulleau, P. P., Gallatin, G. M.: "Line-Edge Roughness Transfer Function and its Application to Determining Mask Effects in EUV Resist Characterization", *Applied Optics*, vol. 42, issue 17, pp. 3390-3397 (2003)

⁶ Vaglio Pret, A., Gronheid, R., Vandeweyer, T., Ishimoto, T., "Line width roughness mitigation in chemically amplified resist by post-litho processes", *Microelectronic Engineering* 87, pp. 1127-1130 (2010)

⁷ Gronheid, R., Vaglio Pret, A., Rathsack, B., Hooge, J., Scheer, S., Nafus, K., Shite, H., Kitano, J., "EUV RLS Performance Tradeoffs for a Polymer Bound PAG Resist", *J. Micro/Nanolith. MEMS MOEMS*, vol. 8, issue 2 (2009)

⁸ Patsis, G. P., Constantoudis, V., Tsirikas, N., Gogolides, E., "Photoresist line-edge roughness analysis using scaling concepts", *J. Microlith., Microfab., Microsyst.*, vol. 3, issue 3, pp. 429-435 (2004)

⁹ Vaglio Pret, A., Gronheid, R., Ishimoto, T., Sekiguchi, K., "Resist roughness evaluation and frequency analysis: metrological challenges and potential solutions for extreme ultraviolet lithography", *J. Micro/Nanolith. MEMS MOEMS*, vol. 9, issue 4 (2010)

¹⁰ Vaglio Pret, A., Gronheid, R., Foubert, P., "Roughness characterization in the frequency domain and linewidth roughness mitigation with post-lithography processes", *J. Micro/Nanolith. MEMS and MOEMS*, vol. 4, issue 4 (2010)

¹¹ Poliakov, P., Blomme, P., Vaglio Pret, A., Miranda Corbalan, M., Van Houdt, J., Dehaene, W., “Bridging Lithography processes and ECC complexity”, IMW (2010), in publication