

A novel methodology for Litho-to-Etch Pattern Fidelity Correction for SADP Process

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ABSTRACT

For 2x nm node semiconductor devices and beyond, more aggressive resolution enhancement techniques (RETs) such as source-mask co-optimization (SMO), litho-etch-litho-etch (LELE) and self-aligned double patterning (SADP) are utilized for the low k1 factor lithography processes. In the SADP process, the pattern fidelity is extremely critical since a slight photoresist (PR) top-loss or profile roughness may impact the later core trim process, due to its sensitivity to environment. During the subsequent sidewall formation and core removal processes, the core trim profile weakness may worsen and induces serious defects that affect the final electrical performance. To predict PR top-loss, a rigorous lithography simulation can provide a reference to modify mask layouts; but it takes a much longer run time and is not capable of full-field mask data preparation.

In this paper, we first brought out an algorithm which utilizes multi-intensity levels from conventional aerial image simulation to assess the physical profile through lithography to core trim etching steps. Subsequently, a novel correction method was utilized to improve the post-etch pattern fidelity without the litho. process window suffering. The results not only matched PR top-loss in rigorous lithography simulation, but also agreed with post-etch wafer data. Furthermore, this methodology can also be incorporated with OPC and post-OPC verification to improve core trim profile and final pattern fidelity at an early stage.

Keywords: double patterning, SADP, core trim, etch loading, pattern density, OPC, photoresist top-loss, pattern fidelity

1. INTRODUCTION

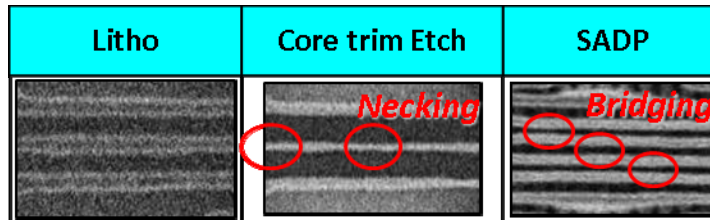
Moore's Law indicates that the number of transistors on a chip doubles approximately every two years [1, 2]. The most effective improvement of resolution is achieved by shorter wavelength of light source (λ) and a lens with high numerical aperture (NA). Nowadays, ArF immersion lithography scanner with NA 1.35 has reached the fundamental resolution limit of 40 nm half pitch and beyond. In order to abide by Moore's law, the industry has to extend the ArF immersion technology due to the extreme ultraviolet (EUV) lithography still not ready for manufacturing owing to the bottlenecks in light sources, masks, and resist materials. For 2x nm node semiconductor devices and beyond, more aggressive resolution enhancement techniques (RETs) such as source-mask co-optimization (SMO), litho-etch-litho-etch (LELE) and self-aligned double patterning (SADP) processes are utilized for the low k1 factor lithography processes. Self-aligned double patterning has been widely adopted to push pattern resolution limit to sub-2x nm technology node.

Several researches have revealed the options of core materials such as a hard mask core for forming the spacers on a hard mask pattern [3], a bottom anti-reflectivity coating (BARC) or spin-on carbon (SOC) core for forming spacers on a BARC or SOC pattern [4, 5], and a photoresist (PR) core for forming spacers directly on the PR pattern [6-8]. All in all, the resist core is the most cost-effective. SADP has the advantage of excellent overlay performance in pitch splitting, and is very useful for one-dimensional (1-D) patterns in memory applications; but for two-dimensional (2-D) random layout, it is still challenging. Due to its limitation, SADP might require extra masks for 2-D random layout application. Therefore, the pattern decomposition for 2-D random logic layout has been studied in several reports [9-13].

However, few studies have reported that the pattern fidelity is extremely critical since a slight PR top-loss or profile roughness may also impact the later core trim process due to its sensitivity to environment in SADP process,

especially for a 2-D random layout. The core trim profile weakness may be enhanced and can induce serious necking and bridging defects during the subsequent sidewall formation and core removal processes, affecting the final electrical performance (Table 1). A rigorous lithography simulation can predict PR top-loss and provide a reference to modify mask layouts; but it would take a much longer run time and not be suitable to full-field mask data preparation.

Table 1 Pattern fidelity from Lithography, core trim etch to SADP steps.



The purpose of this study was to bring out an algorithm which utilizes multi-intensity levels from conventional aerial image simulation to assess the physical profile through lithography to core trim etching steps. Subsequently, a novel correction method would be utilized to improve the post-etch pattern fidelity without the litho. process window suffering.

The results of this study not only matched PR top-loss in rigorous lithography simulation but also agreed with post-etch wafer data. Furthermore, this methodology can also be incorporated with OPC and post-OPC verification to improve core trim profile and final pattern fidelity at an early stage.

2. METHOD

2.1 SADP Introduction

Figure 1 illustrates the process flow of self-aligned double patterning. PR patterns were formed firstly by the lithography process using ArF immersion scanner. Secondly, core patterns were fabricated by dry etch trimming in the hard mask-1 etching step, followed by spacer film deposition with ALD. Spacer open and core removal were performed by dry and wet etching processes. Finally, hard mask-2 patterns were defined with pitch halved from the original PR patterns.

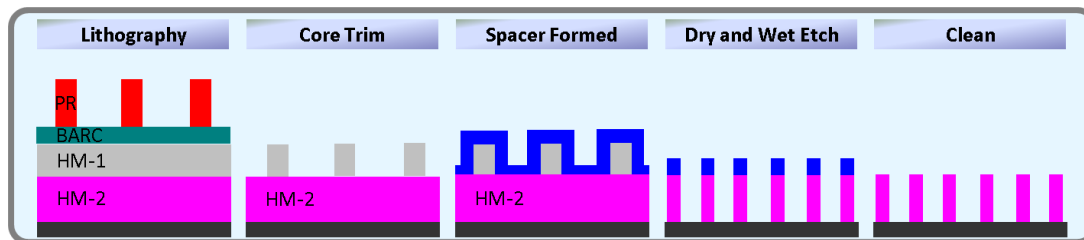


Figure 1 Process flow of self-aligned double patterning (SADP).

2.2 Rigorous Resist-model

An industry standard rigorous PR model for PR top-loss studying is used for simulation (by PROLITH) to predict different mask environment (different layout modification) on how the PR profile relates to the induced defect and how to then solve the weak point problem on wafer. A rigorous PR model we used that covers exposure, PEB (Post Exposure Bake) and developing lithography process. There is a well-calibrated photo-resist rigorous model in PROLITH database and the vendor also validated the photoresist base line parameters from measurement. We combined these two sets of data to match wafer output for getting a suitable model for PR profile simulation with an accurate PR top-loss effect!

Mainly, the factors manipulated in the PR top-loss in rigorous PR model are R_{min} & develop contrast R_n . Some other exposure and PEB parameters will be impacted, but only minorly. We split R_{min} & develop contrast R_n to study the relative PR top-loss effect (Figure 2).

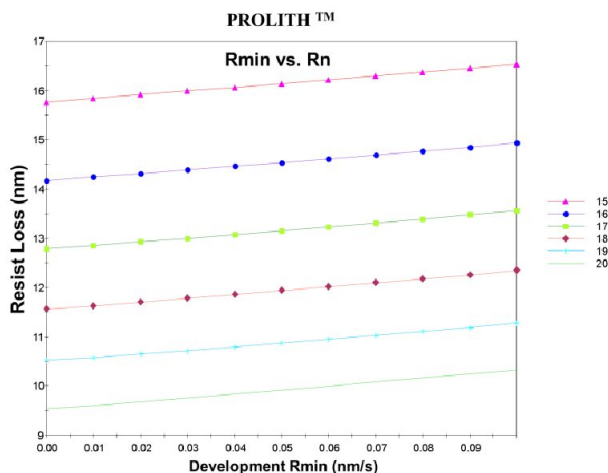


Figure 2 Study of Rmin vs. develop contrast Rn for top-loss effect (Line).

Using the common Original Mack Developing Model:

$$R(M) = R_{\max} \frac{(a+1)(1-M)^n}{a+(1-M)^n} + R_{\min}$$

$$a = \frac{n+1}{n-1} (1-M_{th})^n$$

Where:

R_{\max} is the value in the Development Rmax (nm/s) field.

n is the value in the Development n field.

R_{\min} is the value in the Development Rmin (nm/s) field.

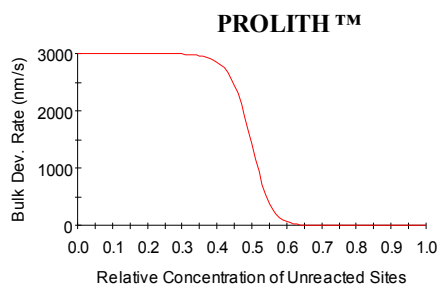
M_{th} is the value in the Development Mth field.

With a larger Rmin & a smaller develop contrast Rn results in a higher value of PR top-loss. The opposite leads to a lower value of PR top-loss. This rigorous PR model simulation can illustrate the PR top-loss' relation to the core trim weak point that we do not check out until after viewing the lithography top-down PR fidelity.

2.3 Advanced Fidelity Correction Method

From the rigorous PR model simulation, PR thickness variation can be found at the cutlines PA1~PA5 and Y (Figure 7) which correlates closely with post-etch weak points. This implies that PR top-loss influences post-etch pattern profile, and can't be easily ignored. Utilizing the rigorous PR model is effective in detecting these weak points at the local area; but is somewhat impractical to apply at full-chip verification. Hence, a simple but efficient method is needed.

Basic aerial image intensity indices such as maximum intensity (I_{\max}) and minimum intensity (I_{\min}) are often used to examine unexpected printing results due to their correlation to physical simulation. Figure 3 shows the post-etch wafer data, together with the simulated lithography contour. Figure 3(a) shows the intensity distribution of the layout of interest though cutline PA3. It reveals higher I_{\min} at the central PR line which implies higher possibility of PR top-loss and this matches the rigorous model simulation result. However, a single cutline is not adequate enough to understand the situation throughout the entire PR line pattern.



A cutline Y is hence used to monitor the overall performance of whole PR line (Figure 3(b)). It's found that although the simulated contour between the two dash lines segment is straight, the intensity distribution reveals obvious differences in intensity, so a potential risk at PR thickness variation through the line segment is suspected. Utilizing single or multiple cutline is workable to find out potential risks at critical features; but it still lacks sufficient information to do layout modification for pattern fidelity correction.

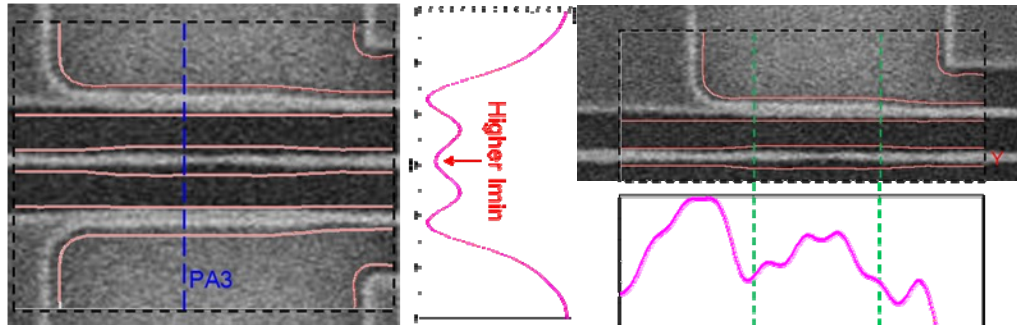


Figure 3 (a) The intensity distribution through cutline PA3 shows a local higher I_{min} at the central line which indicates top-loss risk (left), (b) The intensity distribution through cutline Y shows obvious intensity difference between the green lines, which implies possible PR thickness non-uniformity (right).

Since I_{min} can be correlated with PR thickness, the PR thickness variation at a local region can also be specified by the similar concept to express etch weak points more straightforwardly. For example, a local intensity distribution map with two extra intensity levels is shown in Figure 4. I_{th} is the simulated contour with a threshold intensity to match the lithography target, IL1 and IL2 are simulated contour with intensity level-1 and intensity level-2. From Figure 4, the simulated critical dimension (CD) shows high consistency at the middle of the central line, this represents a smooth profile at the lithography step. In contrast, CD shrinkage can be found at IL2 contour which are marked with red circles. This represents a higher local I_{min} and implies the possibility of a local PR top-loss that induces defects after the etch process. With the introduction of multi-intensity levels, the PR thickness variation or top-loss can be specified and can be taken as a methodology to detect post-etch weak points.

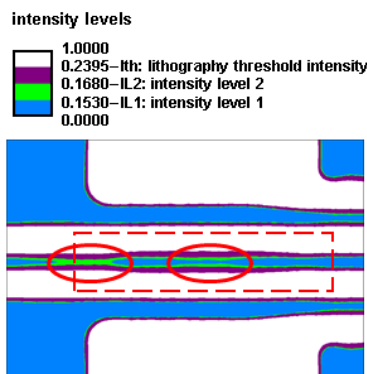


Figure 4 2-D intensity distribution represented by multi-intensity levels. I_{th} shows the simulated litho. contour, IL1 and IL2 show two extra intensity levels to detect potential post-etch weak points. With the two levels, the potential risk points are detected and marked.

Furthermore, the multi-intensity levels are offering hints for layout modification to eliminate the predicted post-etch weak points. As shown in Figure 5, since the distribution map of selective multi-intensity levels is also contoured and is a CD based information, the post-etch profile variation can be eased by adjusting the layout to achieve a smoother contour for each intensity levels, just like the concepts of OPC modification. Firstly, the contour of respective intensity levels are divided into several segments $S_1, S_2, S_3, \dots, S_n$, then the segments are given reasonable specifications according to the lithography and etch target. Afterwards, the edges of each segment are adjusted to make each intensity levels comply with the defined specifications.

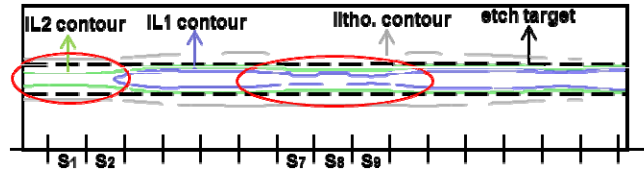


Figure 5 Simulated litho., IL1 and IL2 contours presented in a gray, a purple, and a green color respectively. Modification to correct potential risk points (marked red) can be done by adjusting each segment to achieve the defined specification.

3. RESULT

3.1 Rigorous Resist-model Profile

Simulation PR profile on the Hot-Spot (HS) to explain the failure: the result of five metrology cutline along with the HS region and also the two cutline of Pad area to compare PR top-loss. The simulation result showed that the larger PR top-loss induced the failure. There are three different layout modifications: from the original layout is to achieve for the lithography target but failed after the etching process; then simply enlarge line width (add positive bias on original layout), resulting over correction failure! An inventive novel methodology solved this HS problem getting a suitable PR top-loss just between the two failed layout modifications. It's a very sensitive-factor in which we discovered the difference between these three types of layout modification, the PR top-loss value is not a big difference to each other, but the result showed a good evidence for a reasonable trend that can explain the failure scenario. Metrology cutline position and simulation PR top-loss result (also PR profile) are show in Figure 6 and Figure 7.

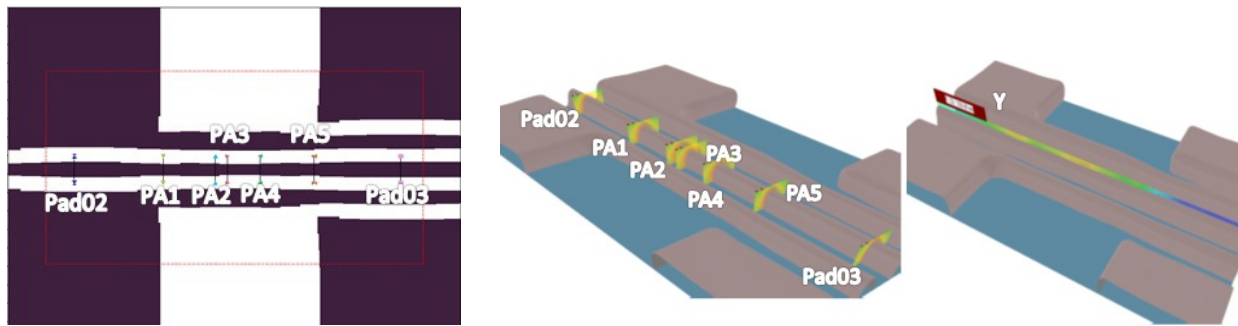


Figure 6 2-D and 3-D view of simulation for both X&Y direction of Metrology Cutline position on weak point (PA1~PA5; Pad02~Pad03; Y).

PR Top-loss (nm)						
Anchor Pattern PR Top-loss = 17.1nm						
Outline	Original		Simply Enlarge		Novel Methodology	
	PR Profile	PR Top-loss	PR Profile	PR Top-loss	PR Profile	PR Top-loss
PA1		23.2		23.3		18.2
PA2		20.1		15.3		19.2
PA3		21.7		16.4		18.1
PA4		21.8		16.1		19.4
PA5		18.9		19		15
Pad02		15.4		15.4		17
Pad03		12.2		12.2		13.9
Y						

Figure 7 All the Metrology Cutline PR profile and PR top-loss result

We can demonstrate that (PA1~PA5 and Y-cutline) the PR CD & PR top-loss uniformity of the inventive novel methodology is better than the others using the PROLITH rigorous PR model simulation.

3.2 Local Etching Loading

Local etching loading has become non-negligible for pattern definition in SADP process at advanced nodes. The PR top-loss in different HS is different in the local position. It will affect the pattern CD and fidelity after core trim etch. In the regular pattern, etching bias is constant but in the irregular pattern (HS) etching bias is not constant and varies at different lithography CD targets (Figure 8). As a consequence, local etching loading must be taken into consideration for lithography-to-etch pattern fidelity correction.

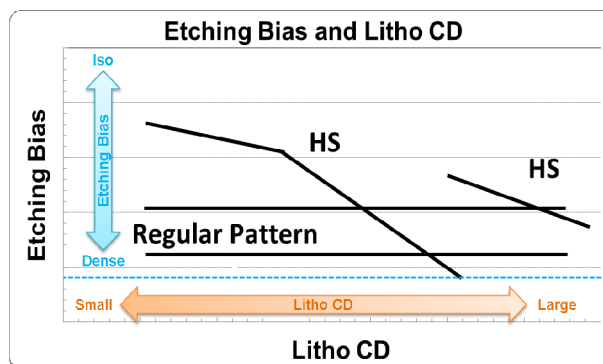


Figure 8 Local Etching Loading at different local position and Litho CD

3.3 Litho-to-Etch Correction

The validation results of the aforementioned methodology are shown in Figure 8. Figure 9(a) left shows the simulation result representing multi-intensity levels. The images from left to right are the original layout, modified layout by simply enlarging central line width, and layout modified by the novel methodology. The original layout shows two weak points indicated clearly by IL1 and IL2 contoured necking, and the weak points are also found at post-etch wafer data (Figure 9(b) left), as predicted. The weak points are then enhanced during following processes causing pattern bridge after SADP process as shown in Figure 9(c) left; the modification result by simply enlarging central line width shows over-corrected result since the IL1 contour is too thick at the central line (Figure 9(a) center). From the post-etch data, the too thick central line is also found as predicted (Figure 9(b) center). This also makes the later formed central spacers to be too close to outer spacers resulting in bridging defects after full SADP process (Figure 9(c) center). On the contrary, the simulation result by the novel methodology shows not only a smoother IL1 contour than the original layout, but also a more reasonable line width than simply enlarging the line width (Figure 9(a) right). The post-etch data also shows a smoother line profile as expected (Figure 9(b) right). Finally, the corresponding full SADP process result shows that the pattern fidelity can be improved as expected (Figure 9(c) right)

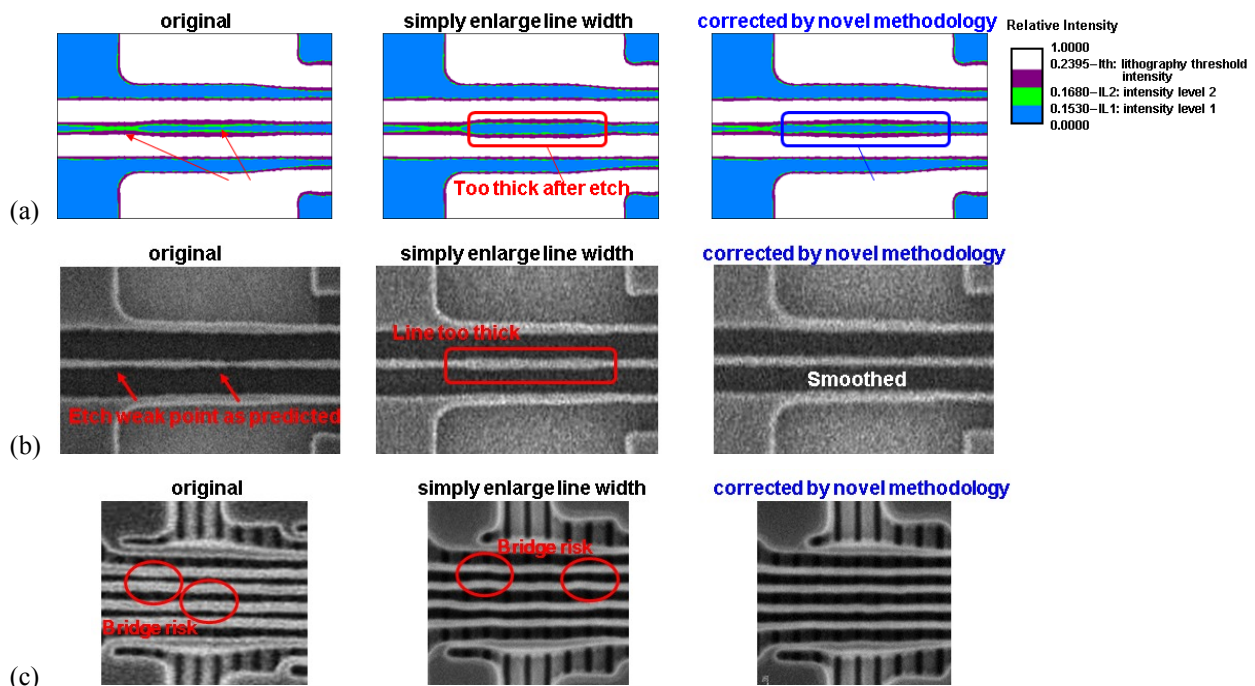


Figure 9 The images from left to right present the original layout (left), layout modified by simply enlarging line width (center), and the layout corrected by the novel methodology (right). (a)The simulated results built by multi-intensity levels. (b)The core trim post-etch data. (c)The final result after full SADP processes

Besides, these steps can be incorporated into the general OPC flow as shown in Figure 10: After lithography verification at the general OPC flow, a post-etch verification can be done from steps A1 to A4. If the verification result is acceptable, the layout can be taped out normally for mask making. Otherwise, the procedure will enter A5 to do layout modification for correcting post-etch weak points. After the correction is processed, the modified layout will do lithography verification again to ensure an acceptable lithography performance.

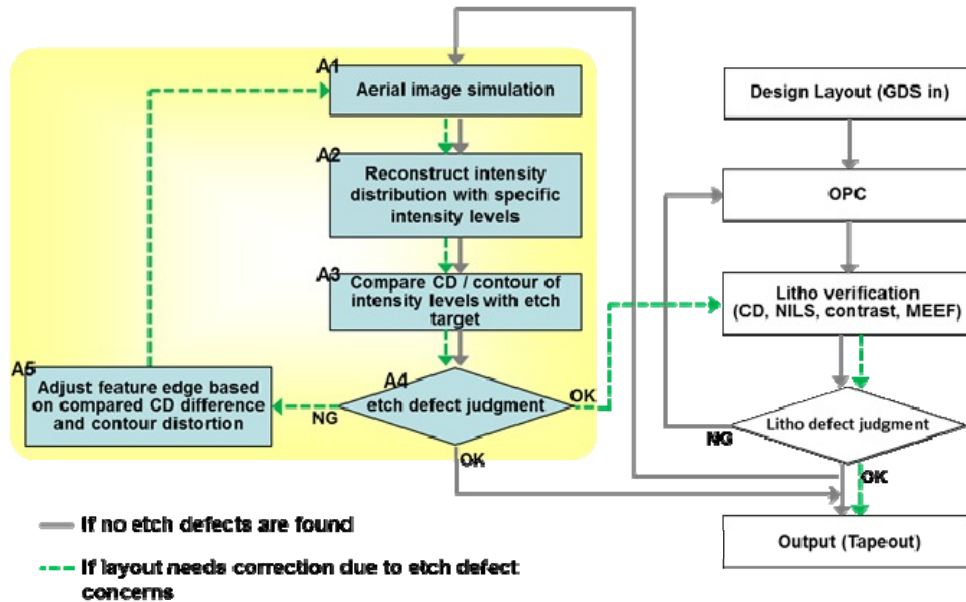


Figure 10: The OPC flow in combination with the novel methodology for post-etch weak point detection and correction (the extra route is shown in green dash line).

4. CONCLUSION

In conclusion, we proposed a novel methodology that utilizes multi-intensity levels from conventional aerial image simulation to reconstruct a 2-D intensity distribution to assess pattern profile at core trim etch steps. The methodology not only detects post-etch weak points at an early stage before mask tape out, but also offers information to do layout modification to correct post-etch weak points. It is simple and efficient compared to rigorous lithography simulation. The validation result not only matched PR top-loss in rigorous lithography simulation, but also agreed with post-etch wafer data. Last of all, this methodology can be combined with the general OPC flow to improve etch profile fidelity without the lithography process window suffering.

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