Yield Enhancement in Stripper Process and related process using SensArray HighTemp wafer

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Abstract – HT-350 is a novel product to do process temperature in-situ measurement. Temperature is the most important factor in strip process. In this paper, HT-350 data helps customer a lot in process maintenances and recipe tuning. The final goal is process monitor and control fab off-line etching rate (ER) chart by HT-350 wafer.

Keywords—HT-350; Strip; Remote plasma; Oxidation layer; Wafer break

I. INTRODUCTION

Semiconductor device geometry becomes smaller and smaller in advanced IC manufacturing. Minor process inconsistencies could cause significant impacts on yield in advanced node devices [1]. The strip process is unique in its front-end line integration. Upon removal of the photoresist and advanced patterning layers with the dry etch method, the exposed silicon or metal surface can be significantly modified by plasma. The modification of post-implant Si could introduce losses in conductivity and degradation/ inconsistency in the transistor's electrical performance [2]. Modification of the metal gate would also cause a loss in the gate work function. Since the strip process is temperature sensitive, the importance of understanding the effect of temperature has been well recognized [3]. In this collaboration with a customer, we obtain a real-time wafer level temperature measurement with the HT-350 product, and demonstrate the contribution of temperature monitoring for yield and production.

II. HT-350 DESIGN

Table 1 summarizes the performance results of two different products. The traditional wire-thermal couple (TC) wafer is used in the higher temperature measurement of the thin film process. The wireless etch temp (ET) product is mainly used in etch processes having a lower temperature range.

TABLE 1 WIRE/WIRELESS COMPARISON

	TC (wire)	ET (wireless)
Temperature	0°C–1100°C	20°C –140°C
Sensors	Up to 34	65
Accuracy	±1.1°C	±0.5°C
Ease of use	No	Yes

The HT-350 (Fig. 1) combines the two products' main features with wireless measurement and higher temperature range operation. The HT-350 heat shield design and lift-one spacing protect the CPU/ memory/ battery, and the module height including the wafer itself is less than 6 mm (Fig. 2). There are a total of 21 sensors on the wafer surface and its accuracy is ±1°C.

FIG. 1 HT-350 WAFER

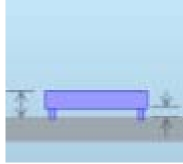

FIG. 2 MODULE HEIGHT CROSS-SECTION IMAGE

III. ISSUES BACKGROUND

The customer's strip process has two main tool types for 28/40 nm production: the Tool A and the Tool B. The user experienced two issues in production as follows:

1) In the SPC oxidation layer chart, the Tool B had better control than the Tool A. This aspect impacts dopant uniformity, so Tool B achieved good wafer-to-wafer WAT distribution.
2) After the production strip process, wafers then begin the wet batch clean process, during which many break.

IV. HT-350 IN SPC CONTROL ISSUES

This oxidation layer SPEC tightens process control by only 20±2 Å. The red line in Fig. 3(schematic diagram) shows the Tool A results and the green line shows that for the Tool B. It is clear that the Tool A tool SPC performance was worse than that of the Tool B, but the user had no basis for explaining these results.

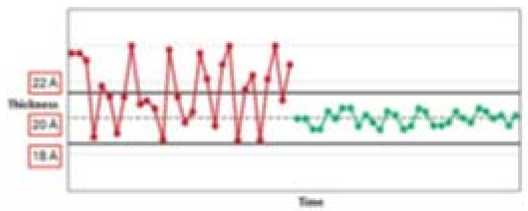

FIG. 3. OXIDATION LAYER THICKNESS SPC CHART (SCHEMATIC DIAGRAM)

After collecting HT-350 data in the Tool A and Tool B chambers during the cooling step, the Tool B tool shows uniformly better temperatures (Fig. 4).

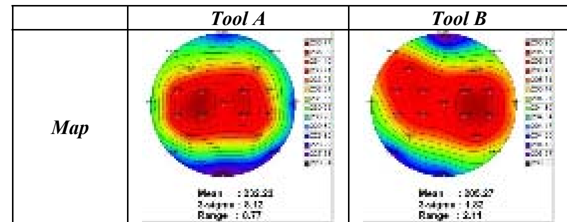

TABLE 2. HT-350 COOLING MAPS FOR TOOL A AND TOOL B TOOLS

Fig. 4 shows that temperature uniformity is strongly correlated with oxidation layer distribution. Better cooling temperature uniformity corresponds to a better oxide layer distribution [4]. Also, the transfer chamber (TM) gas is another factor: in the Tool A cooling step, the inside TM consists of air, but in the Tool B it is N2.

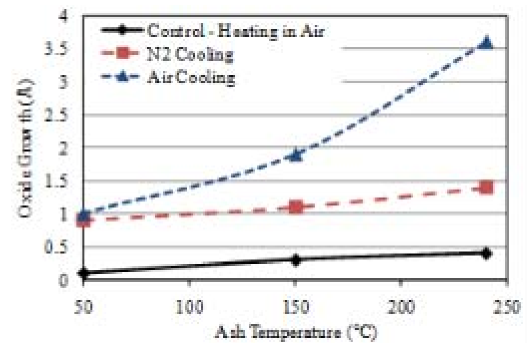

FIG. 4. OXIDATION LAYER THICKNESS CORRELATED WITH TEMPERATURE

At times, after the strip process, the wafers would be sent to an implant process for implanting dopants of different elements. Oxidation layer uniformity impacts the dopant depth inside the wafer. As you can see in Fig. 5 (schematic diagram), there are different resistance profile distribution behaviors in one lot by the two different tools.

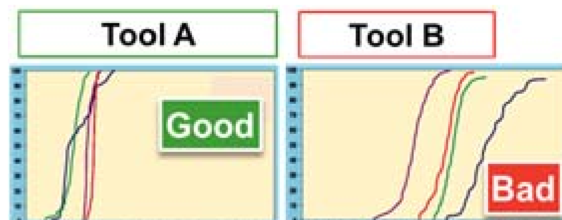

FIG. 5. RESISTANCE PROFILE DISTRIBUTIONS (SCHEMATIC DIAGRAM)

V. HT-350 IN WAFER BREAK ISSUES

At times, after the strip process, the wafers begin a batch cleaning process to better remove their bottom residue. But during the batch cleaning process, the wafers may all be broken (Fig. 6).

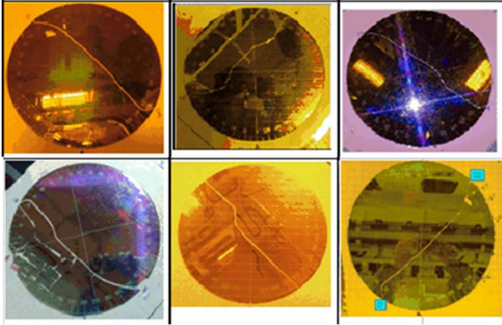

FIG. 6 WAFER BREAKS POST-BATCH CLEANING PROCESS

After collecting HT-350 data for the full process loop, we used robots to touch wafers after the strip process, and discovered one obvious cold spot, as shown in Fig. 7.

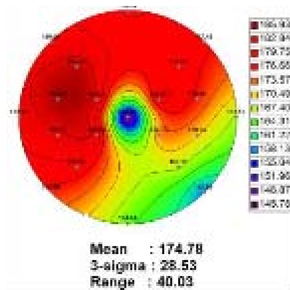

FIG. 7. HT-350 MAP OF COLD SPOT

Then we generated thermal stress inside the wafers, and found one side to be cold and the other to be hot, as shown in Fig. 8.

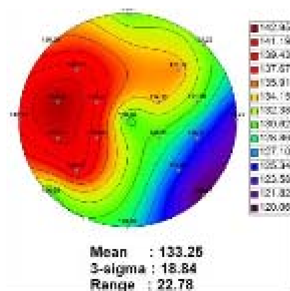

FIG. 8. HT-350 MAP

The cold and hot boundary directions on the distribution map indicate the same wafer break. Because the strip process tool doesn't have an aligner, the wafer break pictures must be rotated to match.

VI. HT-350 IN PROCESSES BELOW 28 NM

After seeing that the two issues were highly correlated on the HT-350 map, we collected more data to identify factors affecting the process below 28 nm. The first factor is the "PR ER off-line chart control" (Fig. 9).

FIG. 9. PR ER CHART

The PR ER chart doesn't show good control, and the strongest peak is temperature. Prior to the HT-350, users had only a heater offset, and conducted a pi-run of one PR wafer to confirm results, which wasted time and resources. With the HT-350, the user collects HT-350 data first. The HT-350 data shows the true wafer surface temperature, then sets the wafer temperature on the basis of the heater offset table. Customers easily save time and the SPC chart guides them to the proper SPEC.

The second factor is the "recipe behavior differences in different generations."

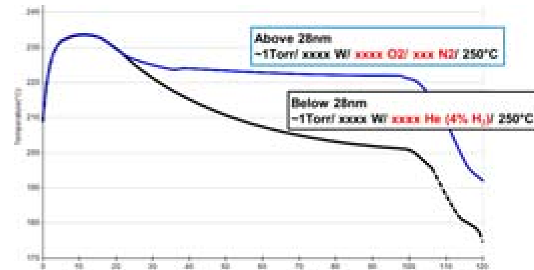

FIG. 10. TEMPERATURE PROFILE IN DIFFERENT GENERATIONS

O_2 is a powerful gas in the strip process, but for processes below 28 nm, O_2 introduces a huge amount of oxidation to the high K/metal gate. So, the gas recipe changes to helium. We found the temperature profile to drop more than in the old generation (Fig. 10), but since temperature drops only to above 200°C at the end of the process, the customer has little or no concern about it.

The third factor is the "recipe optimization and gain in wafer throughput."

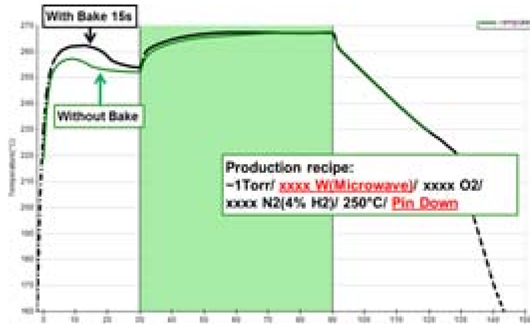

FIG. 11. TEMPERATURE PROFILE FOR DIFFERENT RECIPE SETTINGS

Previously, the customer believed they could use a one-bake step prior to the process, with the idea of increasing the PR removal rate. The thinking was that if the wafer was allowed to pre-heat first, then after the process began, the process could start at a higher temperature. But after collecting HT-350 data, we found that this bake step benefitted the process very little (Fig. 11). The temperature, with or without the bake step, would drop to around 250°C after the chamber pumped down. After the process was completed, the wafers' temperature was at the same level. So the 15 s bake step does not affect the process. As such, the customer plans to remove this step and thereby gain more wafer throughput.

VII. SUMMARY

This paper describes the first application of the advanced foundry fabrication by the HT-350. Using the HT-350 product helped to resolve customer chamber matching, address production yield issues in wafer breaks, and facilitate recipe optimization. This collaboration with our customer proved highly valuable, with respect to the HT-350 product, in process control and yield improvement.

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