Etch process monitoring possibilities and root cause analysis

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***Abstract*— Tilt of the shallow trench isolation on the wafer edge with the radial signature is a known issue for all technology nodes. Presence of this tilt was proven by cross-sectional TEM measurements. For advanced nodes, starting from 28 nm, this tilt becomes one of the crucial yield-killer strongly influencing the performance of the edge dies. If this tilt is not corrected for, overlay values of all FEOL layers will include an error on the wafer edge which leads to low performance of the devices and possibly yield loss. The etch process is thought to be responsible for the tilt, however even for the simplest stack the mechanism and reason of the tilt is not clear. The ability to monitor this tilt in production opens a way for understanding this mechanism and even eliminate the root cause. In this paper we will present the opportunity to measure with Spectroscopic critical dimension (SCD) and Overlay-Accuracy flags the asymmetry of tilted etch structures as well as identify the possible root cause of the tilt by monitoring the nanotopography before and after the etch process.**

Keywords*— *Advanced Metrology, Advanced Equipment and Materials Processes, Advanced Process Control, Equipment Reliability and Productivity Enhancements, Enabling Technologies and Innovative Devices, Yield Enhancement/Learning

I. INTRODUCTION

The fact that the overlay (OVL) error is not only determined by lithography has previously been reported in the semiconductor industry [1-7]. As a result of tightening the OVL budget while improving the scanner performance, the influence of pre- and post-lithography processes starts to play a crucial role in the alignment of structures on the chip. OVL values after lithography are well controlled and corrected in production. However the “real” OVL which defines the performance of the chip could significantly vary from lithography OVL due to process related effects, like etch driven scaling [1, 3] and non-uniform stress [2]. This might lead to the significant OVL bias between lithography and etch. Radial scaling signatures of this bias could be driven by a non-homogeneous tilt of etched structures. The presence of this tilt was proven by cross-sectional electron microscope measurements [1, 5-7]. For Shallow Trench Isolation (STI) structures this tilt on the wafer edge is well known for all technology nodes. For advanced nodes starting from 28nm and below, STI tilt becomes one of the dominating process variations impacting the OVL budget at the edge of the wafer and strongly influencing the performance of the edge dies. If this tilt is not corrected for, OVL values for all FEOL layers include an error on the wafer edge which leads to low performance of the devices potentially causing yield loss. The etch process is thought to be responsible for the tilt, however even for the simplest stack the mechanism and reason of the tilt is not completely understood, and its influence on OVL was not taken into consideration [8]. Moreover, radial signatures of the OVL bias have been observed for MOL and BEOL layers also. The ability to monitor the tilt in production could be an enabler to understand the mechanism, to correct for it and ideally to eliminate it by finding and fixing the root cause.

In this paper we demonstrate an inline, non-destructive, fast and accurate application for monitoring the etch-induced tilt and its signature across the wafer. Two different metrology approaches were used and compared:

- Measuring the tilt using a spectroscopic critical dimensions (SCD) model
- Accuracy flags (specific algorithms) based on Archer images of OVL targets [9,10].

As the first step, we used a SCD metrology tool (KLA-Tencor SpectraCD XTr) to measure the angle of the asymmetric tilt of the structure and define its resolution. As the second step, we used an OVL metrology tool (KLA-Tencor Archer 500 LCM) to define the accuracy flag which is mostly sensitive to the asymmetric tilt. Finally we examined the correlation between both, the accuracy flag and the SCD measured tilt wafer signatures.

Additionally, we evaluated if the wafer geometry measured by the KLA-Tencor WaferSight PWG (Patterned Wafer Geometry) tool could give us a hint for the root cause of the etch-induced tilt on the wafer edge. This technique was used in this work because of its suitability for monitoring stress-induced wafer shape changes as well as topography, both factors which can impact the etching process.

Using the data obtained from SCD and OVL, we checked for correlation between any component of wafer geometry and the tilt signature. The SCD-tilt measurements were done using new function of KLA-Tencor’s AcuShape SCD modelling software

(SW) which enables modeling of tilted structures. The evaluation of different OVL accuracy flags was done on AIM target images collected on an Archer500LCM tool.

II. EXPERIMENTAL DETAILS

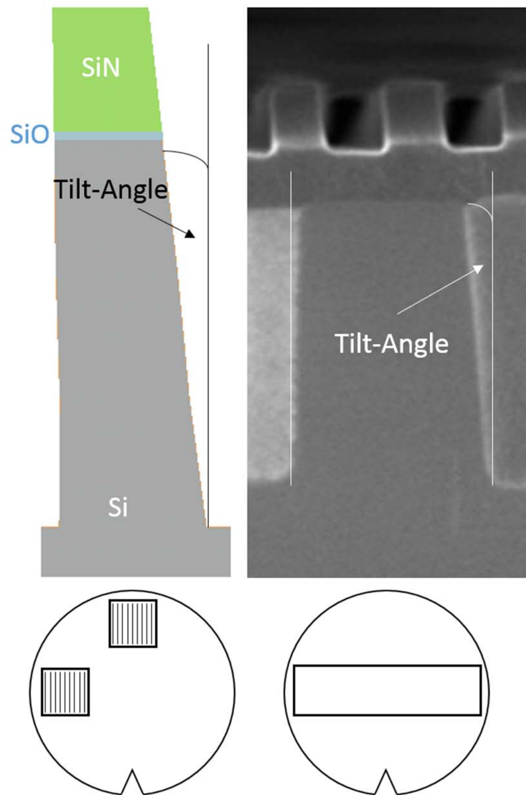

Figure 1 - Upper left side shows the modeled asymmetric building block of AcuShape™ SW indicating the measured tilt angle. Upper right side shows a TEM image indicating the tilt of a STI structure. Lower left side diagram shows the orientation of the targets across the wafer and the lower right side diagram, the area where the tilt was measured and from where the correlation plot was produced.

The KLA-Tencor SpectraCD-XTR optical CD/metrology tool with AcuShape™ modelling software was used to record the experimental SCD data. Spectroscopic ellipsometry was chosen as experimental technique. AcuShape™3.1 has, additional to the conventional building blocks (BB), new BB`s which allow the user to model tilted structures easily without much effort. In Figure 1 the AcuShape™-SCD-model used is shown illustrating the possibility to model the tilt of the STI-structure. The side wall angle in the model describes the symmetric part of the target whereas the tilt angle describes the asymmetric one. The measured wafers had test pads with the STI structure across the wafer to get the behavior of the tilt on the whole wafer.

To enable OVL measurements of the STI structure, the wafer was processed until the next litho step. The OVL measurements were performed between this mask referenced to the etched STI layer. Images of the target were collected on the KLA-Tencor overlay (Archer500LCM) tool measuring four targets per field and all fields on the wafer. The asymmetry of the etched (reference) part of the target was addressed by the detailed accuracy flags (metrics) analysis using an off-line SW. This SW analyzes the greyscale values of the overlay-target kernels by various mathematical criteria.

Figure 2 sketches the way how the OVL target image is analyzed. In this study the inner and outer part of the target represents etched STI layer and the resist of the next litho step respectively. Each part of the target consists of four regions of interest (ROI): two for each direction (X and Y). To probe the accuracy of the target, the gray scale profile of the ROI image undergoes various transformations using different algorithms. Each algorithm provides a value, called accuracy flag that characterizes the specific asymmetry of the target. All 50 available flags were examined to assess its correlation to the tilt signature.

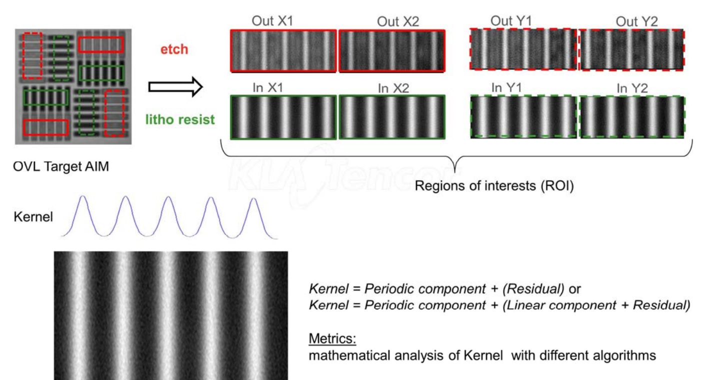

Figure 2 – Asymmetry monitoring with overlay target. Target is separated into the regions of interest (ROIs). The gray scale of the ROIs is analyzed using different mathematical algorithms resulting in accuracy key values.

The KLA-Tencor WaferSight-PWG tool was used to measure the actual shape of the wafer before and after the etch process to identify possible root causes for the tilt. The PWG-tool is an optical interferometry system which measures both the front surface and back surface height of patterned wafers at high throughput and at high resolution (~3.5 million points per wafer). During the measurement, the wafer is held gently in a vertical position by three-point edge gripping. This is to minimize any gravitational distortions so that the wafer retains its original free-standing shape. The most important parameter was the measured backside nanotopography (NT). The NT is obtained by applying a high pass Double Gaussian filter on the high resolution surface height measured: the resulting topography map keeps only spatial wavelengths that are less than 20 mm. By monitoring both the front and back surface nanotopography, PWG can provide unique insight into how the frontside etching process may also be impacted by the topography of the wafer.

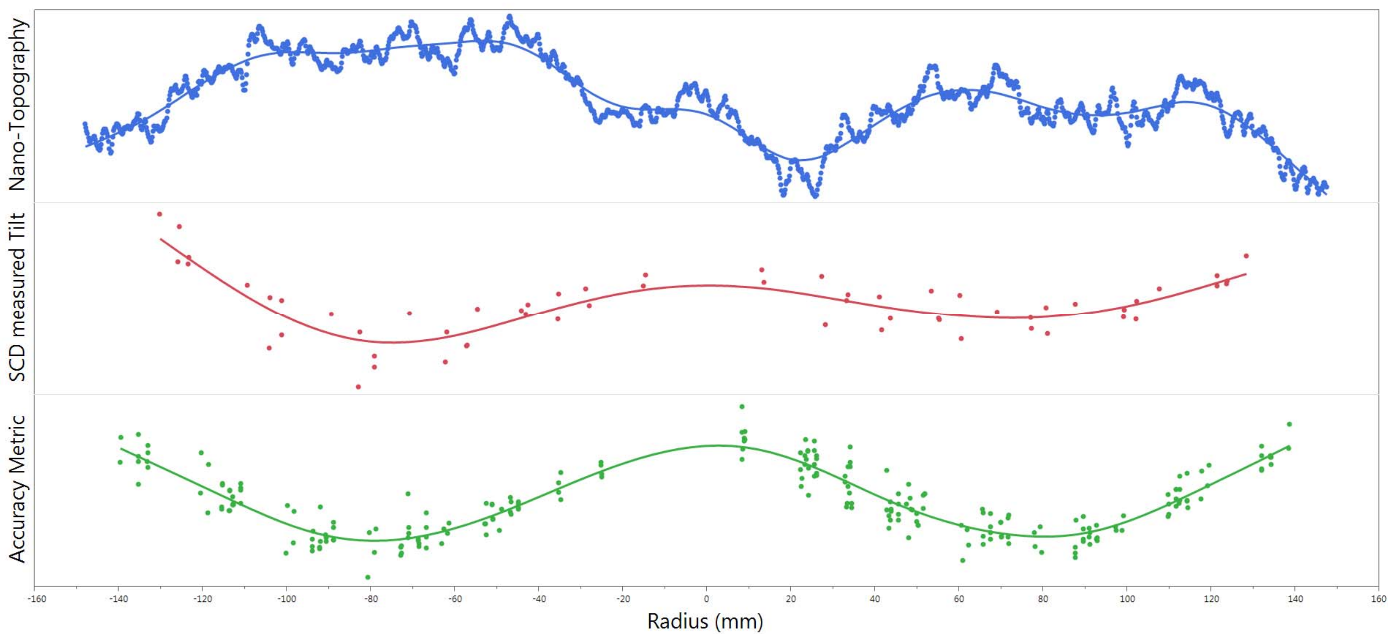

Figure 3 - Radial plot for the Nano-topography (PWG_NT) gained with the PWG tool, the Tilt value gained via SCD and the Overlay accuracy flag AF#2.

III. Results and Discussion

Before the STI etch process the NT of the backside of the wafer was measured by the PWG tool. In the upper panel of Figure 3 the radial behavior of the NT is displayed. As can be seen in Figure 4, the NT shows similar values in the wafer center as well as the wafer edge, whereas larger values were measured in the annular region, indicating that higher amount of material is agglomerated in this so-called “donut” region.

After the STI etch step this wafer was measured in the SCD tool using the tilt model introduced in Figure 1. Since the available SCD targets have only lines directed parallel to the notch (only in Y direction), the tilt model is generally sensitive to the X tilt. Thus, the trustful model results are located in the rectangular area around the wafer diameter in the X direction (see lower right panel of Figure 1). This limitation was necessary since it is known that the tilting of the lines has radial scaling signature [1]. When looking at the orientation of the targets (see lower left part of Figure 1) it is clear that targets which are not in this area will not be influenced by the radial tilting signature. The middle panel of Figure 3 shows the radial behavior of the tilt for this rectangular area of the wafer. The tilt at the wafer center as well as at the extreme edge shows comparable values whereas in the donut area tilting appears to be different. This behavior of the tilt is, as expected, radially symmetric with the symmetry center slightly off the center of the wafer.

After the next litho step, the wafer was measured in the OVL Archer500 LCM tool and the target images were processed in an offline SW for the accuracy flag determination. We chose an accuracy flag which is sensitive to asymmetry in the target investigating just one ROI to detect a possible tilt in the overlay target. In this work we will call this accuracy flag AF#2. Figure 4 plots the wafer map of this accuracy flag for one ROI of the etched part of the target. Other 3 ROIs demonstrates the same radial signature. The currently available metric on the Archer tool, Qmerit [11], was found to be non-sensitive to this kind of asymmetry. The reason is that Qmerit is based on the shift between the center of symmetry of the left and right kernel and their first derivative. The influence of tilt on a kernel results into a difference of amplitude, while Qmerit is sensitive to the differences in phase of the kernel and is well applicable for other kind of target imperfections [12].

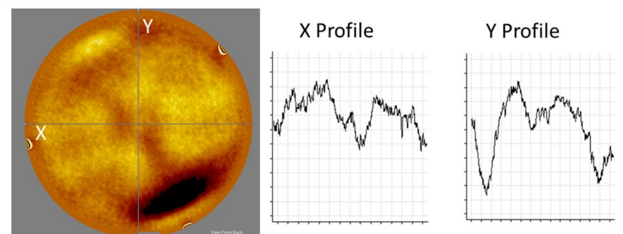

Figure 4 – Backside Nanotopography wafer map showing the donut wafer signature prior to etch step. Additionally shown are line profiles for X- and Y-direction.

Contrary to the SCD Targets, the OVL targets have gratings in both X and Y directions (Figure 2) and can sense the target asymmetry through the whole wafer. However to compare the radial signature of the AF#2 with the SCD measured tilt, the data from the same rectangular wafer region were plotted via radius. The third panel on Figure 3 represents the values of AF#2 over the radius. When AF#2 shows high values (larger asymmetry) the tilt shows also the largest values. The asymmetry/tilt becomes larger with decreasing wafer topography at the backside of the wafer whereas the

asymmetry gets smaller if there is some material on the backside (e.g. as a result from deposition processes or from the original incoming wafer). This correlation between non-uniformity of backside NT and the wafer signature of the tilted etch processes shows that the wafer topography possibly influences the final etch profile.

Correlation between AF#2 and tilt was demonstrated also for other layers in MOL and BEOL for several products. However this data will be not a part of the current manuscript which is focus on STI for one certain product.

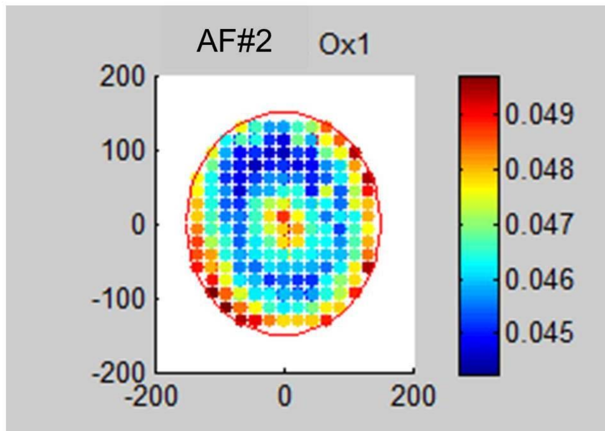

Figure 5 – Wafer map of the accuracy flag AF#2 for the etched part of the target. One ROI is presented as example. The other ROI show the same signature.

IV. CONCLUSIONS

In this paper we demonstrated the possibility to measure and to monitor the tilt of STI structures using two independent measurement techniques. On one hand we used a SCD approach modeling the tilt with the asymmetric BB option of the AcuShape™ SCD modeling SW. On the other hand the Archer500LCM overlay tool does have different accuracy metric which enables the user of this tool to get information about the actual shape of the measured target which includes the possibility to extract information about asymmetry (including the tilt).

Finally we could show that the incoming wafer topography could be responsible for the existence of the tilt evaluated with the PWG tool. Possible root causes can be for example the incoming wafer quality or process residuals of depositions. Further investigations and more detailed analysis are necessary to identify exactly which process contributes to this non-uniformity in backside topography.

V. ACKNOWLEDGEMENT

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